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A fast, direct x-ray detection charge-coupled device

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A charge-coupled device (CCD) capable of 200 Mpixels/s readout has been designed and fabricated on thick, high-resistivity silicon. The CCDs, up to 600 μm thick, are fully depleted, ensuring good infrared to x-ray detection efficiency, together with a small point spread function. High readout speed, with good analog performance, is obtained by the use of a large number of parallel output ports. A set of companion 16-channel custom readout integrated circuits, capable of 15 bits of dynamic range, is used to read out the CCD. A gate array-controlled back end data acquisition system frames and transfers images, as well as provides the CCD clocks. © *2009 American Institute of Physics.* [DOI: 10.1063/1.3187222]

I. INTRODUCTION

Over the past 20 years, the brightness of synchrotron radiation sources has increased by six orders of magnitude, whereas the detectors used in experiments are in many cases unchanged. One of the ubiquitous detectors in synchrotron radiation research is a fiber-coupled phosphor screen, read out by a charge-coupled device (CCD). CCDs have been the scientific imager of choice for more than 3 decades due to their noiseless, efficient charge transfer which allows linear recording of signals over a wide dynamic range. The primary drawback of CCDs is the serial nature of their charge transfer mechanism that tends to be slow.

Our goal was to improve this kind of detector by increasing the CCD readout speed by a factor of 100 while maintaining all of the other excellent characteristics of CCDs. At the same time, fabricating the CCD on thick, high-resistivity silicon opens up the possibility of direct x-ray detection (the CCD is thick enough to absorb essentially all x rays up to 10 keV) as well as improve the point spread function (PSF) (as the CCD is fully depleted, charge is collected solely by drift, without diffusion).

We describe below the design and fabrication of a 96 port CCD on thick, high-resistivity silicon, as well as a companion 16-channel custom readout integrated circuit and the data acquisition system. First results from tests with x rays are presented.

II. CCD DESIGN

Conventional CCDs achieve higher readout speed with increased clock rates and higher digitization frequency. The speed increase results in a corresponding increase in bandwidth, so that the readout noise increases as $f^{1/2}$. With fixed well depth, this results in an $f^{1/2}$ decrease in dynamic range. An alternate way to increase speed is to increase the number of readout ports. In a single port CCD, the image matrix is surrounded by the parallel clock distribution interconnect on two sides and by the output (serial) shift register with a readout port on one side (see Fig. 1). This is commonly extended to two ports by splitting the serial shift register, adding another output port to the other side, and reading half the CCD out of one port and the other half out of the other port. Duplicating this arrangement on the top of the CCD and splitting the parallel clocking directions results in a four port device. One way to further increase the number of readout ports would be to read out every column [column-parallel CCD (Ref. 1)]. When the pixel pitch is narrower than the width of the output stage, this introduces interconnection problems which are insurmountable in most CCD processes. Alternately, one could have many short serial shift registers [almost column-parallel CCD (Ref. 2)], but this requires finding a way to intersperse the output stages into the area occupied by the serial shift register.

The approach we take is the latter: an output stage for every ten columns. In order to fit the output stage in the area of the serial shift register, each ten-column serial shift register is compressed by a short (6 pixels) pitch-adapting taper (see Fig. 2). The pixels in the taper are designed to have the same capacitance (and therefore the same properties) as pixels in the imaging matrix. For reasons described below, the pixel pitch is 30 μm, so that the output pitch is 300 μm. The output stages share a common drain connection for every four outputs, so that together with a V_{DD} pad, the resulting 240 μm pad pitch allows simple wire bonding. In conventional scientific CCDs, reset and output V_{DD} pads are not shared in order to minimize cross-talk, whereas for the high density of this CCD, individual power pads would lead to a prohibitive number of power supplies.

The CCD was fabricated in a process originally developed at LBNL,[3] where a conventional CCD structure is grown on a high-resistivity silicon wafer. The high resistivity allows the complete volume of the imaging matrix to be

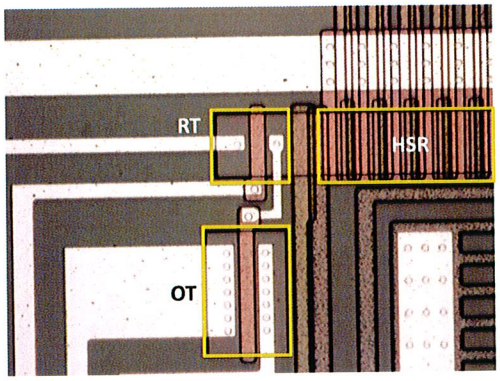

FIG. 1. (Color online) Microphotograph of the output stage of a typical three-phase CCD. The serial shift register is labeled HSR, and the reset and output transistors are labeled RT and OT, respectively.

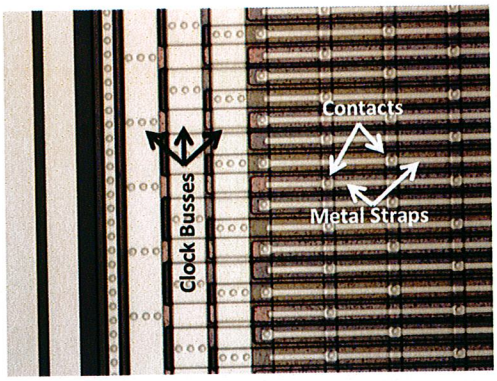

FIG. 3. (Color online) Microphotograph of metal-strapped CCD gates. Each polysilicon gate is covered with metal and contacted (over the channel stop) every other pixel.

depleted so that all of the charge is collected and diffusion is minimized. In addition, the entrance window (backside) is specially designed[4] to present a minimum of dead material while maintaining good conductivity. This allows the same device to simultaneously be optically sensitive (with excellent blue and red quantum efficiencies), sensitive to x rays from the VUV to ~10 keV, and sensitive to low energy electrons.

The time needed to read out a CCD with $N_X N_Y$ pixels having m output ports on the top and bottom each is $T = (N_Y/2)[T_V + (N_X/m)T_H]$, where T_V is the parallel clock time and T_H is the time to serially shift one column and digitize the output. In a three-phase CCD (like this one) three parallel clocks must be toggled during time T_V, so that T_V should be a small fraction of $(N_X/m)T_H$ in order to not introduce significant dead time. Unlike the serial (mini)shift registers, the parallel clock gates traverse the width of the CCD. The polysilicon gate resistivity is three orders of magnitude higher than that of aluminum. For normal (slow) CCD readout, this is not a concern, but at high speeds the RC time constant (R from the polysilicon gate resistivity and C from the combination of gate overlap and channel capacitance) can make T_V prohibitively long. For this reason, the gates have been metal strapped, whereby (as shown in Fig. 3) each polysilicon gate is covered with metal, and contacted every second channel stop. The lithographic tolerances needed for the contact and metal etching steps result in a minimum metal-strapped pixel pitch of about 25 μm.

The CCD lot was fabricated on high-resistivity 6 in. wafers, 675 μm thick by Dalsa Semiconductor. Dalsa provides the front-end processing (implants, polysilicon gates), after which thinning, backside processing, and metallization are performed at the LBNL Microsystems Laboratory. The backside processing involves high temperatures so the aluminum metallization must be performed last. A few control wafers were fully processed by Dalsa (i.e., including metallization). Those wafers can only be frontside illuminated and are 675 μm thick. CCDs processed at LBNL can be front side or back side illuminated and for this lot were thinned to 200 μm.

III. CCD SIGNAL PROCESSING INTEGRATED CIRCUIT

The high density of analog outputs from the CCD makes discrete readout impractical. We have therefore developed a custom integrated circuit, fCRIC, to acquire and digitize the CCD signals. The fCRIC is based upon a floating-point architecture developed at LBNL (Ref. 5) and is shown in Fig. 4. The CCD output is ac coupled to the input stage, where the signal is amplified and converted from single ended to differential. The differential output voltage signal is then integrated by a differential multislope integrator which functions as follows: Initially, all switches are open, so that the

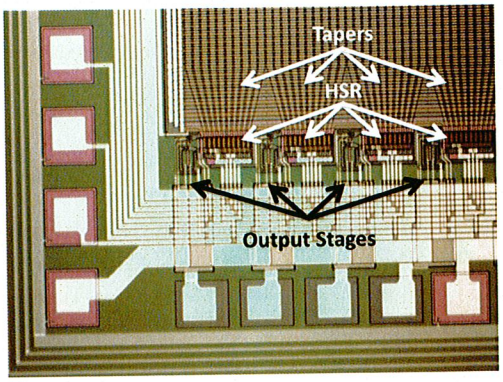

FIG. 2. (Color online) Microphotograph of the output stages of the almost column-parallel CCD. The constant-area tapers are visible, as are the 10 pixel miniserial shift registers labeled HSR. Output stages are nestled between the shift registers.

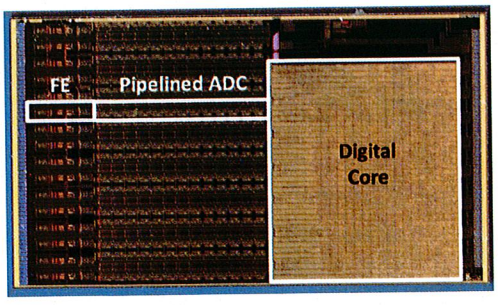

FIG. 4. (Color online) Photograph of fCRIC readout integrated circuit. For one of the 16 identical channels, the analog front end, labeled FE, is shown, along with its pipelined ADC. The digital core, common to the chip, is also shown.

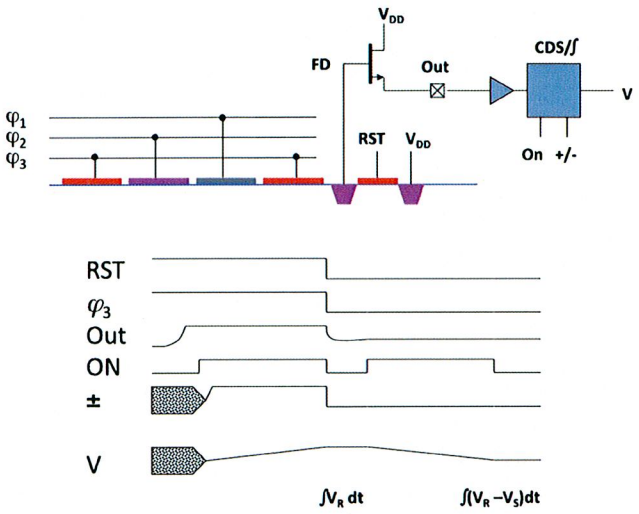

FIG. 5. (Color online) Schematic of the end of the serial shift register, output stage, and fCRIC along with the timing diagram. While RST and ON are high, the reset level is integrated. The signal charge to be integrated is then clocked onto the floating diffusion, the sign of integration is changed, and the signal level is integrated for the same amount of time as the reset level. The resulting voltage to be digitized is thus $\propto\int(V_R-V_S)dt$.

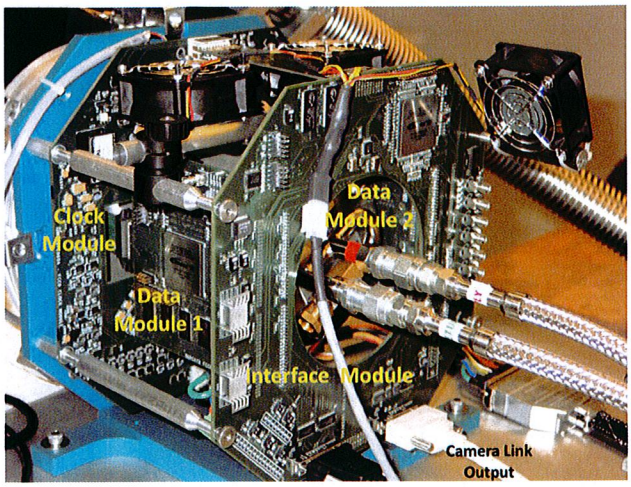

FIG. 6. (Color online) Back end readout showing the clock, data, and interface modules.

feedback capacitance is C. If the integrator output exceeds a preset threshold, then capacitors $3C$ are switched in. The feedback capacitance now goes from C to $4C$, which means that the gain has been reduced by a factor of 4. Similarly, if the integrator output again exceeds the preset threshold, then capacitors $4C$ are switched on. With a feedback capacitance of $8C$ defined as unity gain, the three effective gains are 8, 2, and 1. As shown in the timing diagram in Fig. 5, first the reset level of the CCD is integrated. The sign of the integration is now changed, and the signal level is integrated. This subtraction of the reset level from the signal level is known as correlated double sampling and is used in CCDs to reduce low frequency noise.

The analog result, signal reset, is then digitized by a 12 bit pipelined analog to digital converter (ADC). The digital result consists of the ADC mantissa and 2 bits representing the gain (1, 2, or 8). The overall gain has been set so that for a nominal 400 ns signal integration time, 0.5 V at the input of the fCRIC corresponds to the full scale of the ADC. With a typical conversion gain of 3.5 $\mu V/e^-$, full scale corresponds to the $2^{17}e^-$ on the gain 1 scale, $2^{16}e^-$ on the gain 2 scale, and $2^{14}e^-$ on the gain 8 scale. With 12 ADC bits, one analog to digital unit (ADU) thus corresponds to $32e^-$, $16e^-$, or $4e^-$.

The fCRIC contains 16 identical channels sharing a common digital back end. The digital circuitry includes a command decoder and four, serial data output lines, circuitry to assemble the pipelined ADC output into data words, circuitry to self-calibrate the ADCs, and a digital timing generator. The timing generator consists of a number of 8 bit counters, incrementing on a master clock of up to 250 MHz. Each counter controls the transition of the internal timing signals used in the analog signal acquisition and digitization. The 16 channels also share common analog services, including a bandgap voltage reference. The fCRIC was designed and fabricated in commercial 0.25 μm complementary metal oxide semiconductor and measures 4.8×8.3 mm^2.

IV. DIGITAL READOUT AND TIMING CONTROL

The back end electronics, shown in Fig. 6, control the digital readout and the timing of the detector. It consists of an interface module, two data modules, and a clock module. The data from the six fCRICs flow into the two data modules where they are buffered and organized. From the data modules the data are sent to the interface module, which buffers them again and then sends them out a camera link port. The camera link data are received by a Dalsa X64-CL full camera link frame grabber, which is plugged into a PCI 64 slot in a computer. The Dalsa frame grabber is capable of acquisition rates up to 680 Mbits/s and is controlled through a user interface that makes calls to Dalsa's application-programming interface.

The functions of the interface module are to generate all of the CCD clock signals, to provide a method of synchronizing external equipment to the detector, to receive data from the two data modules, and to send the CCD data out to a camera link interface. The logic in the interface module, controlling the CCD clock signals, allows developers to modify many parameters without having to reprogram the field programmable gate array (FPGA). For example, one can change the serial cycle time, the number of pixels read out, the shape of the waveforms, and the clock voltages all from a graphical user interface (GUI) without reprogramming the FPGA.

The functions of the data modules are to receive 12 low voltage differential signaling (LVDS) data streams from three fCRICs, provide a serial bus to program the fCRICs, provide the digital power to the fCRICs, and allow some real time data manipulations. One real time data manipulation is the rearrangement of the data from three fCRICs to match the CCD geometry before sending them to the interface module. The logic implements this descrambling with a ping-

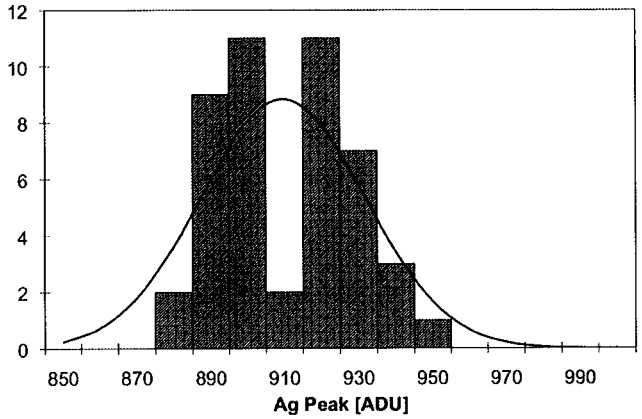

FIG. 7. Histogram and Gaussian fit to the conversion gain for each of the CCD output stages. Plotted is the value in ADU for a fit to the Ag K_α peak for each individual output. The average of all outputs is 909.5 ADU.

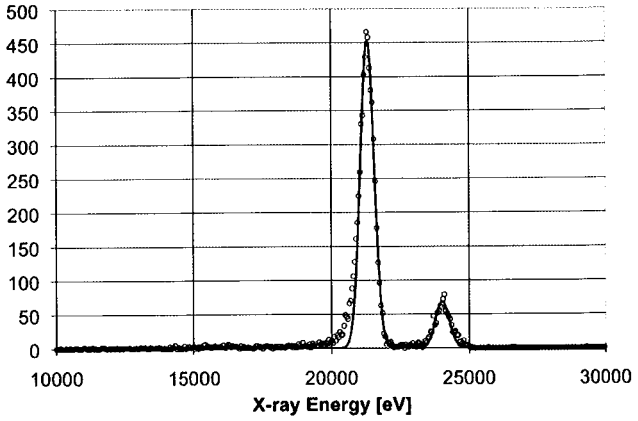

FIG. 8. Histogram and fit for Ag fluorescence photons over the surface of the CCD. The K_α peak has a Gaussian fit width of 250 eV.

pong line buffer: one buffer receives data from the fCRICs while the other buffer is transferring data to the interface module.

The functions of the clock module are to convert the CCD clocks to programmable voltage levels, provide enough current to the clock signals to drive the CCD, provide programmable bias voltages to the CCD, and provide analog power to the fCRICs. The CCD clock signals come from the interface module and are optically isolated from the digital power supply. All of the programmable voltages are set through a serial bus from the interface module and can be modified through the GUI.

V. RESULTS

A prototype CCD with 480×480, 30 μm pixels was fabricated, along with various test devices, including a four port version (20×480 pixels) for use with conventional CCD readout systems. The prototype CCD implements several new design features compared to previous LBNL CCDs: a large number of output stages—48 on each side; use of the constant-area taper, metal strapping, and large (30 μm) pixels. A front-illuminated four port version was characterized first with slow (100 kHz digitization rate) readout in order to assess the performance of the large, metal-strapped pixels and to compare the behavior to previous LBNL CCDs. As the devices are 675 μm thick, there is considerable bulk thermal leakage current, so that measurements must be performed at low temperatures. With ^{55}Fe, the conversion gain was measured at 140 K to be 3.3 $\mu V/e^-$, consistent with expectations. At that temperature, long exposures gave a leakage current of $5e^-/h/pixel$, or 2.5×10^{-17} A/cm^2.

Backside illuminated CCDs thinned to 200 μm have also been characterized on ALS Beamline 5.3.1 (Ref. 6) with fluorescence x rays from thin foils. For all of the subsequent measurements, the CCD was read out at 5 ms/frame. Figure 7 shows a histogram of the gain for each output stage for Ag fluorescence photons (22 keV). At 500 mV full scale on the ×1 gain range, the average peak value of 910 ADU on the ×8 gain range corresponds to a conversion gain of about 2.3 $\mu V/e^-$. This conversion gain is about 1/3 lower than that measured for low-speed operation due to the settling time of the output stage. The single-stage output source follower is biased at 1 mA and has a settling time approaching 1 μs. At low speed, the voltage signal to be integrated is fully settled while integration takes place, but at high speed, it is not, resulting in a lower conversion gain. The output gain uniformity is quite good, as seen in Fig. 7, with a standard deviation of ~3% (which includes the tolerance of the source follower bias resistors, and hence the gain of the output transistor). This demonstrates good matching across the CCD chip.

The spectrum for Ag fluorescence photons, corrected for the output stage gains, is shown in Fig. 8. The measured resolution, 250 eV, is currently read noise limited and will be improved in the next implementation of the readout circuit board. Although the Gaussian PSF for 200 μm fully depleted silicon is around 5 μm, which seems negligible compared to a 30 μm pixel, it is easy to show that for uniform illumination, a 30 μm pixel contains only 75% of the total charge for a 5 μm PSF. This can be seen in Fig. 9, which shows the energy-ordered sum, $S(n)=\Sigma_{i=1}^{n}P_i$, where P_i is the energy recorded in the ith pixel and $P_i>P_{i+1}$. The progression seen in Fig. 9 is consistent with a 5 μm Gaussian PSF. Lastly, different depths of conversion lead to subtle differ-

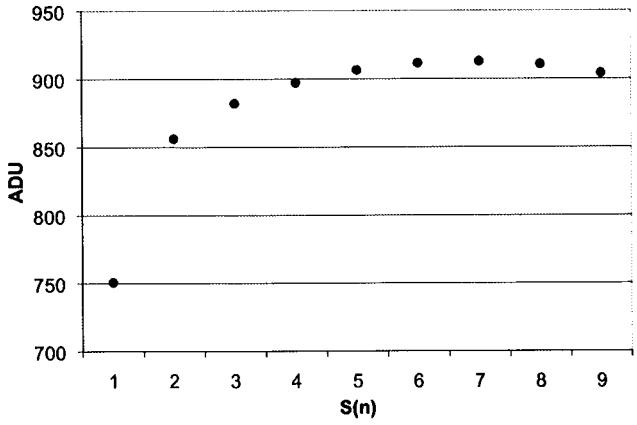

FIG. 9. Charge collected for Ag fluorescence photons for an energy-ordered sum; $S(i)$ is the sum of the ith most energetic pixels.

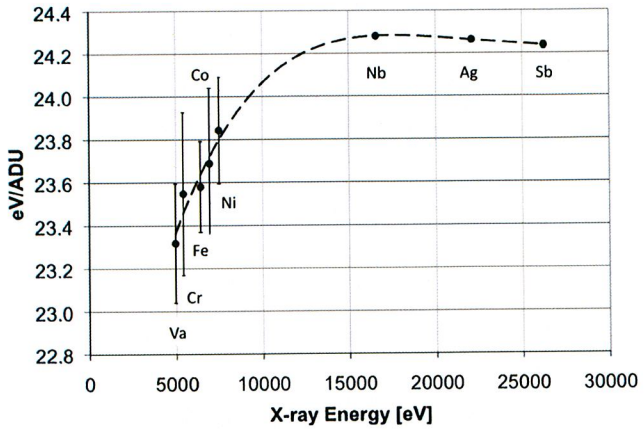

FIG. 10. Calibration constants (eV/ADU) for different x-ray energies.

ences in conversion gain. Figure 10 shows the measured conversion gains as a function of energy, and therefore different average conversion depths.

VI. CONCLUSIONS

A custom CCD, capable of high-speed readout due to multiple output ports, has been fabricated on thick, high-resistivity silicon. This CCD, in addition to high-speed readout for optical photons, has excellent efficiency for direct x-ray detection. To take full advantage of the high performance, a 16-channel custom readout integrated circuit was developed in parallel with the CCD. The complete system includes a digital back end control, clocking, and data acquisition system, capable of acquiring images at 200 frames/s.

The CCD described here was originally developed for optical imaging, to read out, for example, a fiber-coupled phosphor x-ray detector. It is clear, however, that there are several applications of this CCD in direct x-ray detection, such as an imaging energy-measuring (spectroscopic) detector. We will therefore optimize the readout system for direct x-ray detection in a future iteration: the well depth for x rays is significantly less than for optical photons, so a future version will emphasize higher readout speed at the expense of reduced ADC resolution. For applications requiring larger areas, along with an electronic shutter, a 1000×2000 version of this CCD will be fabricated.

ACKNOWLEDGMENTS

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CCD-based vertex detectors

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Abstract

Over the past 20 years, CCD-based vertex detectors have been used to construct some of the most precise 'tracking microscopes' in particle physics. They were initially used by the ACCMOR collaboration for fixed target experiments in CERN, where they enabled the lifetimes of some of the shortest-lived charm particles to be measured precisely. The migration to collider experiments was accomplished in the SLD experiment, where the original 120 Mpixel detector was later upgraded to one with 307 Mpixels. This detector was used in a range of physics studies which exceeded the capability of the LEP detectors, including the most precise limit to date on the B_s mixing parameter. This success, and the high background hit densities that will inevitably be encountered at the future TeV-scale linear collider, have established the need for a silicon pixel-based vertex detector at this machine. The technical options have now been broadened to include a wide range of possible silicon imaging technologies as well as CCDs (monolithic and hybrid silicon pixel devices, DEPFET-based and SOI-based devices). However, there is a good chance that CCD-based detectors, or an architecture derived from CCDs, will still prove to be superior for this application. Groups in Europe, Asia and the USA are working semi-independently on various aspects of this development, with the goal of evaluating prototype detector elements within the next 5 years. If the CCD option is selected for one of the LC detector systems, it is hoped that these groups will join forces to construct the new detector. If the design goals can be achieved, this vertex detector will provide a tool not only for b and c tagging, but also for the measurement of 'vertex charge', allowing discrimination between b and $\bar{b}$ jets, and between c and $\bar{c}$ jets. Given the complex topological nature of much of the potential new physics in the TeV regime (multiple hadronic jets), such a tool could provide the key to unravel novel processes which may be unintelligible at the LHC.

Keywords: Pixel detectors; CCDs; Flavour ID; Linear colliders; Charm quark; Bottom quark

1. Introduction

CCD-based vertex detectors have been used for 20 years for the reconstruction of charm and bottom hadrons as well as tau leptons in fixed target and collider experiments. They have demonstrated the power of silicon pixel devices as tools for heavy flavour physics. Their particular attributes are small pixels, hence excellent spatial and 2-track resolution which permits them to be located close to the interaction point (IP), plus

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unsurpassed material budget (0.6% X_0 per layer in the SLD detector, with each layer providing unambiguous space point determination for each track). To date, CCDs are the only pixel devices to have been used successfully as vertex detectors for heavy flavour physics. Most past and present vertex detectors use silicon microstrips, but this nearly dominant position is about to change, as a variety of silicon pixel devices (CCDs, hybrid active pixel devices (HAPS), monolithic active pixels devices (MAPS), DEPFET arrays etc) are being developed for future experiments [1]. Indeed, we heard in this conference that every future experiment is now planning to use or considering using pixel devices for their next vertex detector. This is due to a combination of factors, such as their extreme rate capability, extreme radiation tolerance, as well as their fundamental attribute of precise and unambiguous space point determination. It is not possible to optimise all these features in the same detector, but it appears that the appropriate choice of pixel technology will provide the preferred vertex detector for a range of conditions: high luminosity hadron colliders, e^+e^- colliders (both B factories and the future TeV-scale linear collider or LC), heavy ion colliders (both RHIC and the LHC) and fixed target experiments.

The use of CCDs for vertex detectors was reviewed 6 years ago [2]. The interested reader is referred to that paper for a description of the early work. In this paper, we avoid covering the old ground, and provide an update to the earlier report. In recent years, the work has been primarily carried out by the GLC vertex collaboration [3], the US Linear Collider vertex collaboration [4] and the LCFI collaboration [5], in all cases directed towards the future LC.

2. Historical background

CCD-based vertex detectors have their roots in the discovery of the charm quark in 1974. After a challenging and only partly successful attempt by the ACCMOR collaboration at CERN to study the hadroproduction of charm particles using a single electron trigger, the emphasis shifted to observing their decays with silicon vertex detectors. The CERN-Munich group pioneered microstrip detectors, while the Rutherford Lab group explored CCDs, which had been invented a few years earlier at Bell Labs [6]. The possibility of using CCDs for particle tracking was explored theoretically in 1981 [7], and their capability for tracking minimum ionising particles with full efficiency and few micron precision was established experimentally in a CERN test beam in 1983 [8]. They were then used for some of the most precise charm lifetime measurements, and physics of charm hadroproduction, by the ACCMOR collaboration [9]. A combination of two CCDs placed 1 and 2 cm beyond the target, followed by 6 planes of microstrip detectors and a multiparticle spectrometer, provided one of the most powerful instruments ever built for the detection and lifetime measurement of charm particles.

Making the giant leap from fixed target experiments to the collider environment was carried out at SLD, for which R&D started in 1984. A first-generation detector of 120 Mpixels [10], installed in 1990, did some very good physics, and this was replaced by a 307 Mpixel upgrade detector [11], which continued till the end of running at SLD, being responsible (among other things) for setting what is still the most sensitive limit on the B_s^0 mixing parameter.

Over the past decade, the three collaborations mentioned above have been engaged in developing a much higher performance vertex detector for the future LC. Each has been exploring different ideas, but it is hoped that they will eventually join forces to produce a vertex detector for one of the experimental facilities (of which there will probably be a total of two) at the future machine. The preferred architecture for the LC vertex detector will depend on which accelerator technology is chosen (room temperature or superconducting RF cavities, the so-called warm and cold options).

From the detector point of view, the most essential difference between the accelerator technologies is the bunch structure of the colliding beams. At the warm machine, a bunch train consists of 190 bunches at 1.4 ns intervals, with a train frequency of 120 Hz. Detector backgrounds are sufficiently low that one can integrate the

signals through the train, reading out between trains. At the cold machine, a bunch train consists of 2820 bunches at 337 ns intervals, with a train frequency of only 5 Hz. Backgrounds integrated through the train would be excessive. For the vertex detector inner layer, it is necessary to divide the train into about 20 time slices, i.e., to read out the detector at approximately 50 μs intervals throughout the train of duration 1 ms.

In neither the warm nor the cold machine option is it guaranteed that CCDs will provide the optimal technology. There is unanimity within the LC community that silicon pixel devices will be used for vertex detectors at this machine, but beyond this there is healthy competition between different architectures (notably CCDs, MAPS, DEPFETs and an SOI-based design), any of which might prove superior. The various R&D groups are planning to develop full-scale prototypes so that choices can be made on the basis of performance achieved in test beams about 5 years from now, assuming that the LC adheres to its aggressive schedule of starting to do physics by 2015. In the meantime, it is not excluded that someone may come up with a revolutionary new idea, better than silicon pixels. In the case of SLC, the preferred vertex detector technology in 1982 was considered to be a rapid cycling bubble chamber! [12] Every technology sooner or later becomes obsolete, and over a 10 year period things can change a great deal. Imaginative young physicists are encouraged to take nothing for granted.

3. Current status of R&D programmes

A CCD in its most basic form consists of an array of pixels of dimensions typically 20 μm square, with the storage of signal charges being defined in one dimension by channel stops, and in the orthogonal dimension by voltages on polysilicon gates which overlay the imaging area. By manipulating these voltages, signal charges are moved physically towards the output node or nodes, where they are transferred onto the gates of voltage-sensing transistors for readout. There are numerous variations on this basic design, some of which have transformed this seemingly sluggish architecture into one which is matched to the requirements of particle physics experiments, and also to high speed photography, where the current record for a 100-frame burst camera is 10^6 frames per second. See Ref. [2] and references therein for a description of CCD operating principles, with particular emphasis on their use in vertex detectors.

The current R&D activities in this field can be divided into four categories. Firstly, physics simulations to define the appropriate technical goals for the TeV-scale linear collider. Secondly, the reduction of the layer thickness well below the figure of $0.6\%X_0$ achieved at SLD, probably to less than $0.1\%X_0$. (By layer thickness, we mean the total material budget, i.e., the thickness of the detector plus support structure, in each of the concentric barrel layers.) Thirdly, to understand the background radiation conditions and to develop a device architecture having sufficient radiation resistance. Fourthly, to design a detector which is compatible with the time structure of the collider. In this respect, the challenges presented by the warm and cold machines are quite different. In this section, we discuss the current status of the work in these four areas.

3.1. *Physics studies, leading to overall detector layout*

Before SLD, it was customary to think of the role of vertex detectors in collider experiments as primarily to permit B tagging, but the SLD experiment demonstrated that much more ambitious physics goals could be achieved. These lessons are particularly relevant to the TeV regime, where multi-jet events will be common, possibly involving production of Higgs bosons, supersymmetric and other heavy particles decaying to $q\bar{q}$ and more complex final states. A vertex detector matched to the physics goals of this environment will tag jets uniquely as light quark, c, $\bar{c}$, b and $\bar{b}$ separately, as well as identifying τ leptons. For example, the study of CP asymmetries in SUSY would require the efficient discrimination between b and $\bar{b}$ jets. The SLD experiment demonstrated that this can be achieved in cases of charged B hadrons by

measuring the vertex charge, and in cases of B_d^0 mesons by measuring the charge dipole [13].

The measurement of vertex charge is the most challenging technical requirement, since it depends on associating each track in a jet either with the primary vertex or with the $b/c/s$ decay chain, including the lowest momentum tracks for which the impact parameter resolution is dominated by multiple scattering in the beampipe and layer-1 of the vertex detector. While it is most important to carry out engineering studies to minimise the thickness of both, the most significant parameter in defining the achievable quality of the vertex charge measurement is the beampipe radius R_b. Here, ongoing dialogue with the accelerator physicists is essential. For example, there are trade-offs between R_b and L^*, the focal length of the final doublet, and it will be necessary to arrive at the correct balance between all parameters which influence the physics performance, such as flavour tagging, calorimetric hermeticity, particle flow information, and so on.

The 'default' vertex detector layout generally studied is sketched in Fig. 1. It consists of five concentric barrels, equally spaced in radius. The long barrels permit 3-hit coverage to $\cos\theta = 0.96$, which is probably as hermetic as will be feasible. Studies have been made of extending the polar angle coverage by means of forward disk detectors, but while these will be valuable in order to improve the tracking hermeticity, they are probably too far from the IP and behind too much material to be much use for flavour tagging. The five barrel layers permit standalone track reconstruction in the vertex detector, which is robust with respect to occasional missing hits due to detector inefficiency, and to high background hit density which will be encountered particularly on the inner layer. Standalone track reconstruction is important for two reasons. As found at SLD, independent track reconstruction in the vertex detector and in the main tracker permits each to be used to understand and correct deficiencies in the other. This is particularly important when commissioning these detectors. Secondly, such a layout is robust in terms of reconstructing low momentum tracks (which may not reach the outer tracker), handling γ conversions (absence of hits in the vertex detector inner layers being an important signature), reconstruction of hyperon and other short-lived strange particle decays, etc. A solenoid field of 4 T is sufficient to control the hit rate from the main background (low energy e^+e^- pairs produced by the beam–beam interaction at the

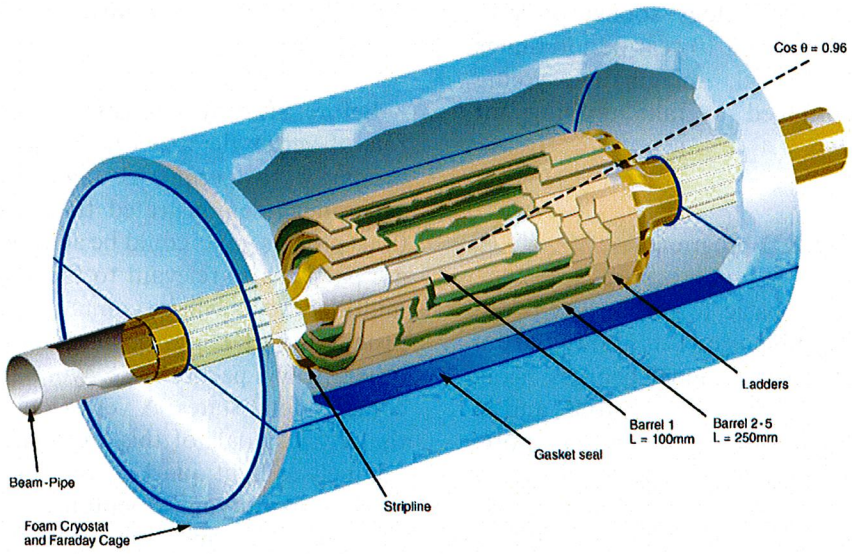

Fig. 1. Isometric view of the vertex detector. The beryllium shell supporting the ladders and stabilising the inner section of thin beampipe is not shown. The foam cryostat of outer radius approximately 12 cm permits operation of the gas-cooled detector at around 200 K or higher.

IP) for an inner layer radius of ~15 mm. It has been demonstrated that the 2-hit resolution of a CCD vertex detector with 20 μm square pixels is sufficient to ensure a low probability of hit merging even on the innermost layer, in the core of high energy hadronic jets.

The relationship between the detector parameters and the physics performance for this vertex detector layout has already been studied for b and charm tagging, based primarily on the topological vertexing program ZVTOP [14] developed for SLD, plus other information from the jet. The results [15] indicate that minimising the radius and thickness of the inner layer is the most important requirement in establishing the highest possible tagging purity for a given efficiency. Not surprisingly, this is most important for charm tagging, due to the shorter lifetimes and lower particle multiplicities in charm decays compared to bottom decays. The evaluation of vertex charge measurement now under way will extend the study to the most challenging physics requirements. As well as impact parameter resolution for low momentum tracks, there is another important reason to minimise the layer thickness. Photon conversions are particularly dangerous, given the goal of jet energy resolution by 'particle flow'. The probability of undesirable photon conversions is directly proportional to the layer thickness, unlike multiple scattering which scales only as the square root of the layer thickness.

3.2. Material budget

CCD tracking detectors use only the epitaxial silicon layer of thickness ~20 μm for signal generation, so the CCDs can in principle be thinned to the edge of this layer. Those used in SLD were thinned to about 150 μm, at which point the unsupported devices become significantly bowed due to internal stresses present in the processed surface of the wafer. In the 'unsupported silicon' option for ladder construction, it was proposed to largely eliminate this bowing and achieve mechanically stable ladders by spring tensioning from one end. Preliminary experimental studies were encouraging, but this approach is now considered to be perhaps overly ambitious, due to the tendency of the devices also to curl significantly across their width, a problem that is difficult to control by tensioning without adding material in the tracking volume.

For this reason, attention has now turned to other options, such as the 'semi-supported' structure, in which the thin silicon is attached to a mechanical substrate (beryllium, carbon fibre or some foam material such as silicon carbide). This substrate can also be thin, and stabilised along its length by tension, but can have sufficient stiffness to resist the tendency of the CCD to curl across its width. There are differential contraction issues to be considered in such assemblies, but these become less severe if the detector can be operated near room temperature, in contrast to the operating temperature of 180 K that was necessary at SLD. The GLC collaboration has been particularly active in exploring the possibility of operation near to room temperature, with encouraging results. As at SLD, it appears that the CCD-based detector can be designed to dissipate on average only some tens of watts in the fiducial volume, so gas cooling will suffice. Piped liquid or evaporative cooling should be avoided if at all possible, since this would impose an excessive contribution to the material budget.

Overall, there is good reason to expect that a design goal of 0.05–0.10% X_0 per layer may be achieved. As in any vertex detector, the material budget beyond the active volume will need to be higher than this. The ends of the CCDs will have readout chips bump-bonded to them, whose power dissipation could possibly necessitate tubes filled with liquid coolant. There will in addition be thin copper–kapton flex circuits carrying power in and digitised sparsified data out, routed along the surface of the beampipe, from each ladder end. For the DAQ system, it is envisaged that LVDS signals will be converted to optical data in the SR masking region where material is no longer so important, and transmitted out with only a single optic fibre being required at each end of the detector.

It is believed that the inner section of the beryllium beampipe of length 10 cm can have a wall thickness as low as 0.4 mm. This is more than enough to withstand the vacuum; the more

stringent requirement comes from stresses during the installation and removal of the beampipe/vertex detector assembly. But here one can take advantage of the fact that beyond the volume used for the very highest precision tracking, the vertex detector ladders are supported by a pair of beryllium half-shells which are clamped to one another and to the outer sections of beampipe. Using this support shell to help stabilise the beampipe permits a reduction in the strength required for the innermost section which is most critical for particle tracking. With a carefully planned installation strategy, it is believed that a wall thickness of 0.4 mm will suffice. A titanium liner is conventionally added to the beampipe to absorb fluorescence X-rays. A useful reduction in material budget where it matters most may be possible by relocating this liner on the surface of the vertex detector support shell. This assumes that the exceptional granularity of the 900 Mpixel vertex detector may make it tolerant of the background due to this flux of soft X-rays, but this question has still to be studied quantitatively.

The currently estimated material budget of the vertex detector is indicated in Fig. 2. For particles with 90° polar angle, the total material inside layer-5 may be kept below 0.5% X_0. This may increase or decrease in future, in the light of ongoing thin ladder R&D programme, together with guidance from the physics studies.

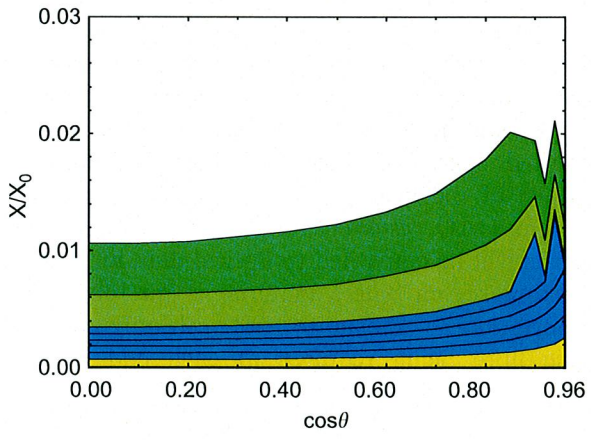

Fig. 2. Material budget as function of polar angle (the plot shows in turn from the bottom the beampipe, each of 5 layers, support shell and cryostat).

3.3. Radiation resistance

The most serious radiation effect in a CCD is bulk damage in the buried channel of the device, the volume in which the signal charge packets are collected and then transferred. In their long journey to the output node of the device (up to 6250 transfers in the outer CCDs of the default design) a charge transfer inefficiency (CTI) of 0.5×10^{-4} would result in a signal loss of up to 27%, which is about the worst one could tolerate before a significant hit inefficiency would be encountered.

The bulk damage at the LC will arise mainly from the e^+e^- pairs produced by the beam–beam interaction at the IP. Though they have typical energies of only ~20 MeV, it has been shown by the GLC group that these electrons will induce cluster damage as well as point defects [16], both of which degrade the CTE. The effects of neutron-induced damage clusters are more serious, but because of the low neutron flux at the interaction region (IR) of the LC (neutrons coming from the beamstrahlung dump and beam dump) they have less overall effect than the pair electrons. Furthermore, the US group has made an interesting discovery regarding neutron damage. They have observed that the trapping of signal charge shows an unexpected time dependence. By observing the effects of individual damage clusters in different pixels, they find that some of them trap signal charge rapidly, as would be expected from a simple calculation based on the known trapping time constant. However, other pixels experience much longer trapping times, up to many milliseconds [17]. A possible explanation could be that these particular damage clusters happen to lie slightly beyond the edge of the storage volume occupied by the signal charge, which can then only be captured when thermal fluctuations drive signal electrons one by one into the trapping volume. Further measurements and full simulations of these effects are now under way, to establish quantitatively whether such an explanation fits all the facts.

Between the GLC and US groups, there are valuable measurements of radiation-induced CTI in a variety of CCD structures. However, these do not translate directly into a lifetime estimate for

the LC vertex detector, because the CTI is a function of a number of negotiable parameters:

- storage volume (so 'notch' or 'supplementary channel' architecture can help) [18],
- clocking rate (faster clocking is beneficial, and is achievable with the column-parallel CCD (CPCCD)),
- operating temperature (lower temperature can dramatically reduce CTI),
- trap occupancy (so the high hit rate from the pair electron background is beneficial).

Preliminary calculations suggest that, as at SLD, it will be possible to design a CCD-based vertex detector with adequate radiation hardness for the LC environment. If the cold machine is selected and the novel architecture discussed in Section 3.4 is adopted, the maximum number of charge transfers would be reduced from 6250 to only 20. Thus a by-product of this approach would be that such devices will have orders of magnitude higher radiation resistance than will be required for the LC. This would open up potential applications in environments where radiation levels are far too hostile for the use of conventional CCDs.

3.4. Timing issues

If the warm machine is selected, conditions for DAQ will be similar to those at SLC. The background hit density integrated through the bunch train (190 bunches at 1.4 ns interval) will be sufficiently modest, even at the innermost layer of the vertex detector, to permit clean standalone track reconstruction in the vertex detector with a negligible level of ambiguous or spoiled (merged) hits. There will be a significant rate of low momentum tracks due to pair electrons, but these particles will also be detected in the forward tracking system, where most of them will be rejected by the fast timing information to be provided by those detectors (silicon hybrid pixels or microstrips). For the vertex detector, the only timing requirement is that it should be read out completely in the 8 ms between bunch trains. This can be accomplished easily with the CPCCD architecture (using a very relaxed 1 MHz clocking rate), or with a more conventional multi-port CCD, having its outputs wire bonded to the readout chip.

A CPCCD readout chip has already been implemented in prototype form by the LCFI collaboration, using a 0.25 μm CMOS process. It has separate channels on 20 μm pitch, each incorporating signal amplifier, correlated double sampling (CDS), 5-bit ADC and on-board memory. The final form of this chip will include data sparsification based on a pixel threshold followed by cluster threshold, as previously used for readout of the 307 Mpixel SLD detector [11]. Data from each readout chip at the ladder ends will be transferred via an LVDS cable to a local electro-optical converter, then out of the detector via a single optical fibre at each end.

If the cold machine is selected, the situation will be more challenging[1]. Background accumulated during the bunch train of 1 ms duration would be 20 times higher than for a bunch train at the warm machine. In order to solve this problem, it was suggested in 1998 to read out the detector repeatedly at 50 μs intervals throughout the train. While this strategy was adopted by the proponents of all silicon pixel technologies considered for the LC vertex detector (CCDs, MAPS, DEPFET, etc), it will in itself create major challenges. What makes this approach dubious is the experience at SLD of beam-induced electromagnetic interference (EMI). It is likely that this will always be worse for a vertex detector at a linear collider than at a circular machine, for several reasons. Firstly, the collimators and beam-position monitors near the final focus induce large wakefields which disrupt the beams. These are tolerable only because the beams pass through them once only—the cumulative effects of such disruptive components in storage rings would be intolerable. This instrumentation is obligatory at the IR of a linear collider in order to meet the challenge of maintaining luminosity with nanometre-sized beams. Secondly, the ceramic feedthroughs and

[1]On 20th August 2004, since writing this paper, ICFA announced that the cold technology has been selected. This means that the vertex detector groups have to deal with the more difficult of the two scenarios.

imperfect coax cables associated with these instruments, as well as apertures for vac pumps, etc, provide escape routes for the RF, as does the thin-walled inner section of the beampipe, which due to the finite skin depth is not perfectly opaque to RF. Thirdly, escaping RF radiation is particularly likely to cause problems for the vertex detector, where the tiny signal charges from about 20 μm active thickness of silicon must be sensed by a high bandwidth circuit with minimal input capacitance—such a circuit being particularly prone to EMI. Furthermore, the pixel-based vertex detector has about 10^9 channels, far more than any other detector in the system, so a tiny fraction of false signals could severely overload the DAQ system. In SLD, the vertex detector electronics was completely disrupted by beam-related pickup for some tens of microseconds after the bunch crossing, and was even then subject to a low level of EMI during the readout period. The former problem was solved by waiting for conditions to settle down, and the latter by using an extension of the correlated double sampling (CDS) technique, the so-called extended row filter [11].

For these reasons, it may be that multiple readout through the bunch train at the cold machine simply will not work. Tests will be carried out in a high energy electron beam at SLAC, and it is possible that the means will be found to suppress EMI to such a level compared to SLD that the problem will be solved. However, this seems unlikely, given the multitude of details on which beam-induced and other sources of EMI depend, and the likelihood that not all these details will be precisely the same in the real IR as in any test facility. Once the real detector is closed up and commissioning begins, it will be almost impossible to investigate such problems, because one cannot run beams with the detector open, as would be needed to operate equipment monitoring EMI conditions close to the IP.

These concerns have led to a variation of the CCD design concept that might be appropriate for the cold machine. We subsequently learned that this concept has already been developed, in the form of a high speed imaging device able to operate at 1 Mframe/s for 100 frames [19], where it is called the 'imaging system with in situ storage' (ISIS). The variant that we are considering for the vertex detector at the cold machine works as follows. The structure (Fig. 3) consists of an array of photogates arranged on a nearly square (slightly trapezoidal) array of dimension 20 μm. These are the charge collection nodes for the imaging pixels in the device. The CCD structure (n-type buried channel) is embedded in a deep p-well. This provides a reflective barrier so that collection of the signal charge by the photogates proceeds by diffusion of electrons generated within the epitaxial layer, as in a conventional CCD. Each photogate is adjacent to a 20-element linear CCD storage register plus conventional charge sensing output circuit. The layout is shown in a more realistic plan view in Fig. 4. Each of the large shaded rectangles at the end of the storage register contains an output circuit, as sketched on the right. Each source follower output of the charge sensing circuit is connected via a row select switch to a busline which runs the full length of the CCD, and is bump-bonded at the edge of the active area to a readout chip having signal inputs at the column pitch of 20 μm, just as in the CPCCD.

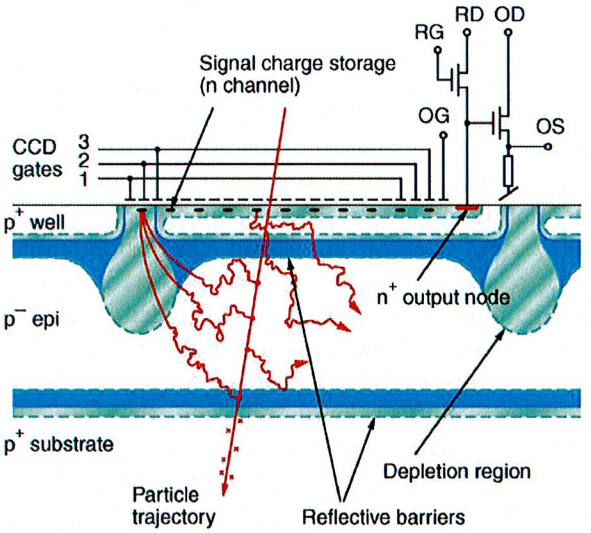

Fig. 3. Sketch of ISIS cross-section (not to scale). Signal charge is reflected from the p^-/p^+ edges above and below the epitaxial layer, so it diffuses within this layer till being collected in the depleted regions beneath the photogates. 10 storage pixels are shown: for the real detector there would be 20.

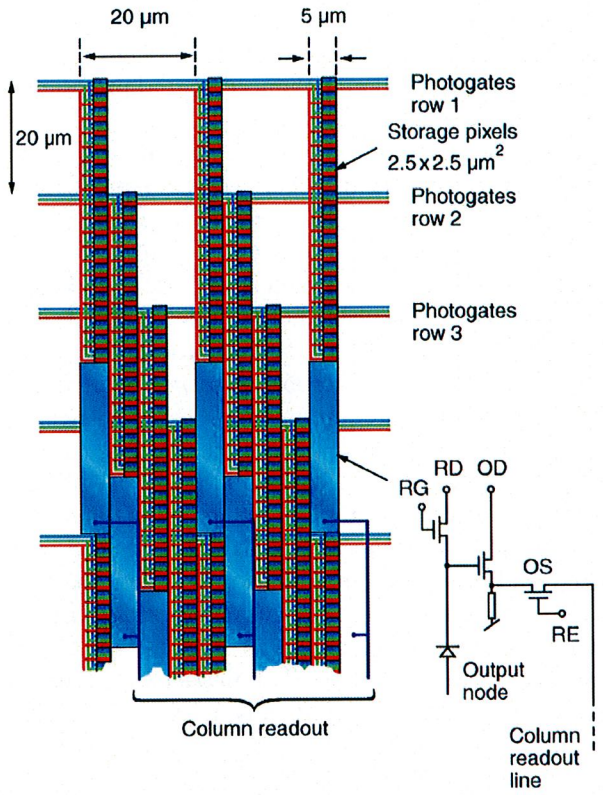

Fig. 4. Top LH corner of ISIS. Photogates are arranged on a regular trapezoidal matrix of elements with 20 μm pitch located at the upper end of each storage register. The tracks to the left of the storage registers represent schematically the buslines which distribute the external potentials to the 3-phase CCD gates. The column readout lines extend over the full length of the device, up to 12.5 cm for the largest devices. During readout, the source follower circuits are connected one row at a time by the Row Enable transistors (RE) to the column readout lines.

During the bunch train, signals accumulated under the photogate are shifted every 50 μs into the adjacent storage register. By the end of the train, the time-sliced signals are stored as charge in the buried channel of the CCD. This method of signal storage is extremely robust, for two reasons. Firstly, to disturb the stored charges, it would be necessary to create ~1 V fluctuations in gate potentials, whereas the signals when converted to voltage amount to typically ~1 mV. Secondly, the CCD gate capacitances are typically some nanofarad, in contrast to the tiny node capacitances of some tens of femifarad. It follows that CCD charge storage provides a factor $\sim 10^6$ greater immunity to EMI than would be achieved by conversion to voltage during the train. This enhanced immunity is achieved by comparison with any of the architectures considered for the LC vertex detector, not only the CCD option. After the end of the bunch train, once the beam-induced RF has died away, the detector is read out. Edge logic, running along the side of the active area, is used to enable one row at a time. Data from all the imaging pixels in that row (20 stored signals/pixel) are read via the output lines, one line per imaging pixel, and sensed by the input circuits on the readout chip. The charge signals which have been accumulated on the CCD nodes for this row are then dumped via the reset drains, while the register clocking is switched to the next row to be read. Reading at a relaxed rate of 1 μs per storage pixel requires a readout time for the largest CCD of $6250 \times 20\,\mu s = 125\,ms$, comfortably within the inter-train period of 200 ms.

It is not necessary to curl up the storage register within the 20 μm square pixel area; it suffices to fit the entire circuit within any rectangular region of area 400 μm^2. This could be achieved with the arrangement sketched in Fig. 4, in which the region allocated to each pixel amounts to $5 \times 80\,\mu m^2$. Discussions with manufacturers of CCDs and CMOS pixel arrays suggest that such a device architecture may be within the capability of currently available technology. However, the desired size of imaging pixels of 20 μm square is challenging. It is not yet clear whether this goal is achievable, nor whether the best hope is by adapting a CCD or CMOS process. A 16×16 element test device with larger pixels, to provide proof of principle for a particle detector, will be manufactured by the end of this year. Should the cold machine be selected, this will be followed by an intensive R&D programme. Given that the timescale for LC physics will be around 2015, one can afford to continue R&D for the vertex detector till about 2010. By that time, an ISIS-type detector with 20 μm pixels will very probably be within the capability of some manufacturers of scientific imaging devices. If the warm machine is selected, the problems are reduced and the next

step will be large CPCCDs with which to assemble full scale prototype ladders.

4. Conclusions

CCD-based vertex detectors have become established over the past 20 years as powerful tools for heavy flavour physics, and for studying high energy processes in which the identification of the leading heavy flavour quarks in jets is important. Although the number of experiments in which they have been used is small, CCDs have delivered the highest performance of any vertex detector architecture. World-wide R&D programmes are currently making excellent progress in the continued evolution of this technology towards a vertex detector at the TeV-scale linear collider.

If the warm machine is selected, the vertex detector requirements will be satisfied by a relatively straightforward extrapolation from the SLD design. Whether to use a CPCCD with every column bump-bonded to the readout chip, or a more conventional multi-port CCD with say 16 outputs wire-bonded, and whether to operate near room temperature or considerably colder, are details which will be decided by the world-wide R&D programme. On the basis of work already completed, one can be confident of a highly competitive vertex detector, which will be well matched to the physics requirements.

For the cold machine, we and all the current technology options face a dilemma, whether or not to hope that multiple readout through the bunch train will be feasible. It may be that studies of EMI in test beams will provide reassurance, but this should not be assumed. For this reason, if the cold option is chosen, we intend to pursue an aggressive R&D programme to establish the ISIS architecture for particle tracking. Since this combines features of both CCD and CMOS imagers, there is not a natural match to the current capabilities of CCD manufacturers. However, we are by no means alone in needing such advanced designs, and several companies are currently developing the necessary capability. Whether essential to overcome EMI or not, the ISIS approach may be preferred due to its other distinct advantages: much reduced power dissipation, greatly enhanced radiation resistance and enhanced spatial precision due to the relaxed readout speed.

The TeV-scale LC may pay enormous physics dividends, such as the discovery of SUSY particles, and precise measurement of their properties. To exploit this potential, a vertex detector (and also an electromagnetic calorimeter) of unprecedented performance will be needed. Through the efforts of the GLC, US and LCFI collaborations, we are well on the way to a vertex detector design that will satisfy these requirements. Once full-scale prototype ladders have been constructed, their tracking efficiency, spatial resolution, etc will be measured in test beams. These results, together with knowledge of the material thickness, readout speed and power dissipation, will be used by the LC experiment collaboration(s) to decide which technology or technologies to include in their overall detector systems. Based on past experience, one can expect ongoing advances in silicon imaging devices, driven partly by very different application areas, to lead to yet more powerful vertex detectors in the future. For this and other reasons, convenient access to the vertex detector, as well as to other equipment at small radius in the heart of the overall detector, will be mandatory. The design concept developed by the SLD collaboration for access to their small-radius equipment looks most attractive. With the endcap detector systems fully opened, the central tracker is transferred to a support rail so that it can be rolled along the beam axis by its full length, thereby exposing the inner tracking system, the vertex detector and other IR instrumentation. By establishing this as a design constraint from the beginning, it will be possible to avoid the problems encountered in some detector systems in which the small-radius detectors were virtually inaccessible without a major shutdown.

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A High Performance CCD on High Resistivity Silicon

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ABSTRACT

In this paper we present new results from the characterization of a fully depleted CCD on high resistivity silicon. The CCD was fabricated at Lawrence Berkeley National Laboratory on a 10-12 KΩ-cm n-type silicon substrate. The CCD is a 200X200 15-μm square pixel array. The high resistivity of the starting material makes it possible to deplete the entire 300 μm thick substrate. This results in improved red and near infrared response compared to a standard CCD. Because the substrate is fully depleted, thinning of the CCD is not required for backside illumination, and the results presented here were obtained with a backside illuminated device. In this paper we present measured quantum efficiency as a function of temperature, and we describe a novel clocking scheme to measure serial charge transfer efficiency. We demonstrate an industrial application in which the CCD is more than an order of magnitude more sensitive than a commercial camera using a standard CCD.

Keywords: CCD, high resistivity, fully depleted, Lick Observatory, Lawrence Berkeley National Laboratory, astronomical

2. INTRODUCTION

The CCD described here was developed for astronomical imaging applications. However, the device characteristics give it many advantages over a standard CCD and therefore it should have potential benefits for other remote sensing applications. The design and fabrication of these devices is described by Holland *et.al,*[1] and initial test results are presented by Stover *et.al*[2]. These CCDs are based on work done at Lawrence Berkeley National Laboratory to develop fully-depleted p-i-n diodes for high-energy physics applications, and all design and fabrication work on the CCDs was carried out there. The starting material for these devices is approximately 10,000 Ω-cm float-zone refined n-type silicon, in 300 μm thick wafers. The CCD employs 15 μm square pixels in a 200x200 array. Standard triple-poly MOS processing was used in fabrication. All testing and characterizations were carried out in the Detector Development Laboratory of the University of California Observatories/Lick Observatory (UCO/Lick) in Santa Cruz, using the standard UCO/Lick data acquisition system[3].

Scientific CCDs have traditionally been fabricated on highly doped p-type silicon, with an active thickness of 25 μm or less. This results in several performance limitations:

1. Illuminated from the front side, quantum efficiency is reduced at all wavelengths by reflections from the polysilicon gate structures.
2. At the blue end of the visible spectrum quantum efficiency for frontside illumination drops to near zero due to absorption in the polysilicon gates.

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3. For red wavelengths ($\lambda > 750$ nm) quantum efficiency drops rapidly because absorption pathlength in silicon becomes large compared to the active thickness of the device.

To overcome the loss of quantum efficiency due to the gate structures on the front of the CCD, the traditional CCD can be thinned to about 20 μm and illuminated from the backside. Excellent results have been achieved with this method. However, the thinning process is difficult and expensive, and the thinned CCD does not improve quantum efficiency in the red. In fact, the thinned CCD starts to become transparent at $\lambda > 750$ nm, and high-order interference fringes are produced by multiply-reflected waves. The accurate calibration of this effect is one of the primary limitations in astronomical imaging at these wavelengths. In p-type silicon the photo-generated electrons tend to be attracted to, and trapped by, the backside surface. Additional processing to modify the backside potential is required to help minimize this problem.

The CCD described here overcomes all of these limitations. Backside illumination is possible without thinning because we can deplete the entire 300 μm thickness of the silicon wafer. With this thickness excellent red response is possible with $\lambda > 1000$nm and interference fringes are eliminated. Because the CCD is fabricated on n-type silicon, holes are the signal carrier, and electron trapping at the backside surface is not a problem.

3. LABORATORY CHARACTERIZATIONS

3.1 Quantum efficiency

The back surface of a thinned p-type silicon CCD naturally develops a potential that attracts and traps photogenerated charge. As a result a newly thinned p-type CCD exhibits very low quantum efficiency. Various processes have been developed to modify the backside surface potential to help reduce the trapping of charge. However, if charge trapping is not eliminated completely, then the quantum efficiency (QE) of the CCD can exhibit instabilities due to a variety of environmental factors including device operating temperature. If this occurs, the QE typically drops as the device temperature is lowered. Since astronomical imaging often requires long exposures on faint sources of light, cooling to about -120°C is required to reduce thermally generated electrons, and it becomes important to maintain high QE when cooled to this temperature.

Since our n-type CCD does not have the problem of charge trapping at the backside surface, we expected better QE stability than is often seen in p-type silicon CCDs. To verify this behavior we measured QE at 10-degree intervals between -90°C and -130°C. Quantum efficiency was measured through a series of narrow-band interference filters, using a calibrated UDT Sensors, Inc. Model PIN UV 100 silicon photodiode as a reference. The results of those measurements are shown in Figure 1. Because there was essentially no QE variation with temperature, we have averaged the measurements at each wavelength and the averages are given in Table 1.

λ (nm)	QE (%)
320	21.3
350	32.4
400	66.7
450	77.7
500	85.7
600	81.7
650	79.4
700	78.0
800	73.4
900	70.7
1000	50.4

TABLE 1. Average measured QE from a series of measurements between -90°C and -130°C.

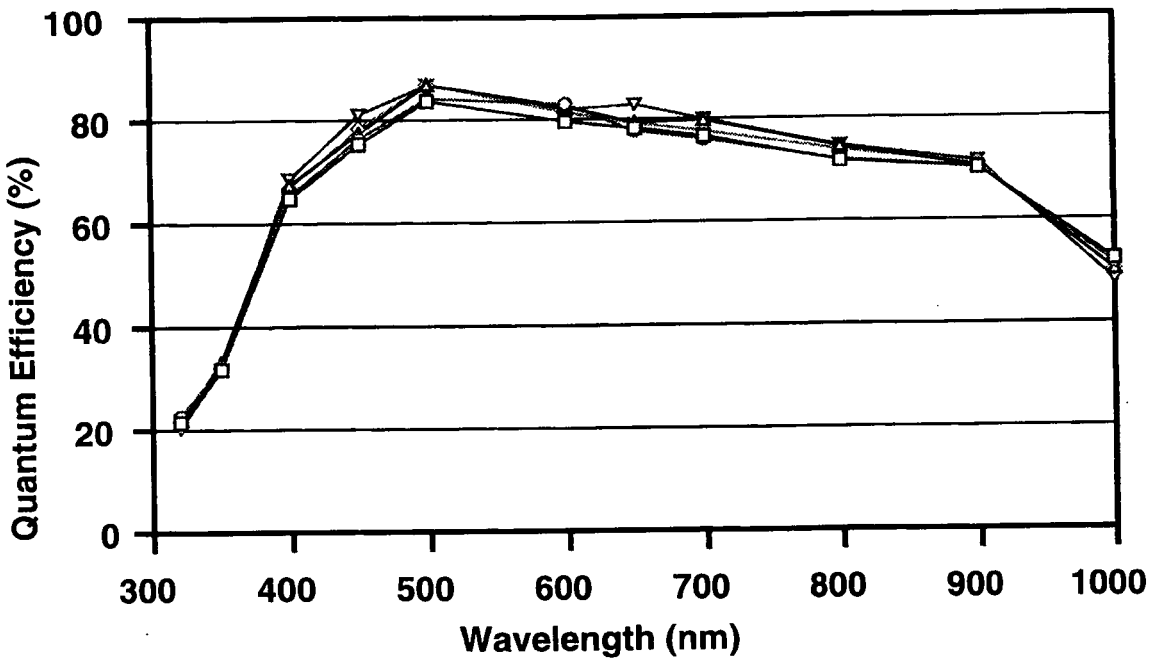

FIGURE 1. Measured quantum efficiency at five temperatures between -90°C and -130°C. N-type silicon has inherent QE stability, as this figure illustrates.

3.2 Charge Transfer Efficiency

The traditional method for measuring charge transfer efficiency (CTE) is to expose the CCD to x-rays from Fe^{55} or a similar source. Each absorbed x-ray produces a charge packet of known size. By analyzing an image of x-ray events it is possible to measure the amount of charge lost in each event. Comparing this charge loss to the number of transfers required to read each event yields the charge transfer efficiency. It is relatively easy to measure 1% charge losses with this method. But with only 200 rows and 200 columns a 1% loss translates into a CTE of 0.99995, which is not very good by modern scientific CCD standards. Because our CCD clearly exhibits better CTE than this, the traditional method is not sensitive enough to yield a reliable measure of CTE. Therefore we developed a new CCD clocking scheme to increase the effective size of the CCD serial register and to measure serial CTE.

We first make an exposure with uniform illumination. One row is transferred into the CCD serial register and then the serial clocks are run to discard all of the image pixels except the last pixel. This single pixel is then shifted back toward the center of the serial register. Next the serial clocks are run to shift the single pixel of charge back and forth in the register many times. Finally, the charge is shifted out of the serial register in normal fashion, amplified, and digitized. The next row is shifted into the serial register and read out in normal serial-clocking fashion. The sequence of special-clocking row and normal-clocking row is repeated 100 times, until the entire CCD is read out. The normal-clocking rows provide an accurate calibration on the original charge level while the 100 special-clocking rows provide data on charge transfer efficiency of the single pixel of charge. To improve the signal-to-noise ratio we may average together up to 10 images before analyzing the results. Analysis of the results is somewhat more complex than the traditional x-ray method because the charge is swept back and forth many

times over the same part of the serial register. If charge is lost while shifting in one direction, it may be picked up again while shifting in the opposite direction. If low-level CTE is different from high-level CTE additional complications can occur. However, all of these effects are simple to model, and an accurate CTE measurement is possible.

Our CTE clocking scheme allows us to sample the CTE at various locations on the serial register by selecting where the single pixel of charge will be placed before the back and forth charge shifting occurs. Using this technique we have found some sections of the serial register which exhibit near perfect CTE (at least 0.999999) and one section with somewhat lower, but still good CTE. This lower CTE might represent a single pixel with a very slight charge-trapping problem, but in our tests we shifted the charge back and forth 20 pixels, so we can't resolve individual pixel locations. We further investigated CTE as a function of signal level. We found that the near perfect sections of the serial register were uniformly excellent at all signal levels. The section with lower CTE exhibited variations with signal level, and that variation is shown in Figure 2. All of our measurements were made at a temperature between -120°C and -130°C.

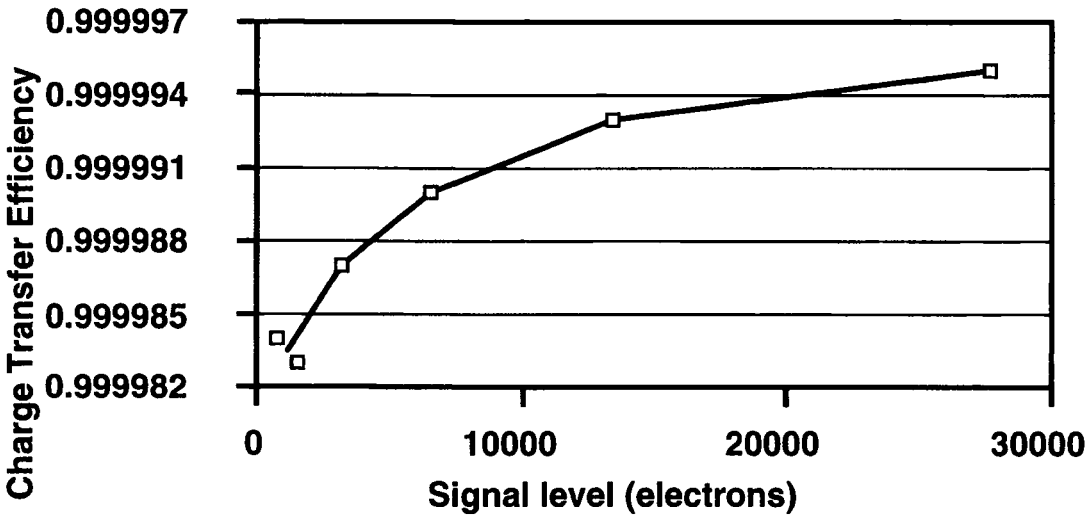

FIGURE 2. CTE is shown as a function of signal level for one section of the CCD serial register.

Note that the CTE shown in Figure 2 is still very good and occurs in one small section of the serial register. This probably would not even be noticed using the traditional x-ray method for measuring CTE.

3.3 Industrial Monitoring Application

We have been working with an integrated circuit manufacturer on an application of the high-resistivity CCD which takes advantage of its excellent response in the near infrared part of the spectrum. In this application we are imaging an integrated circuit which is normally mounted face-down so that none of the components of the integrated circuit are visible at optical wavelengths. To monitor the operation of the device we image the light emissions from various junctions on the integrated circuit. Only those wavelengths that can pass through the 500 μm thick substrate emerge from the integrated circuit. However, because of the good QE of the high-resistivity CCD, we are able to image these emissions relatively easily. Figure 3 shows three frames of the same integrated circuit under various operating conditions. The frame on the left shows the typical pattern of emissions after the device is first powered up. The middle frame shows the pattern of emissions when the circuit's "chip select" signal is de-asserted. The right frame shows the emissions when "chip select" is re-asserted. Had this been a properly

functioning device the left and right frames would look identical. In fact they do not, and the difference between the two frames gives the integrated circuit design engineers valuable clues as to why this device is not working.

The circuit manufacturer tried this same experiment using a commercial camera with a standard scientific CCD. He estimates that the high-resistivity CCD is at least forty (40) times faster than the CCD in his commercial camera. This increase in sensitivity greatly reduces the time required to examine a single circuit, and the reduced exposure time makes it practical to check every device on the production line.

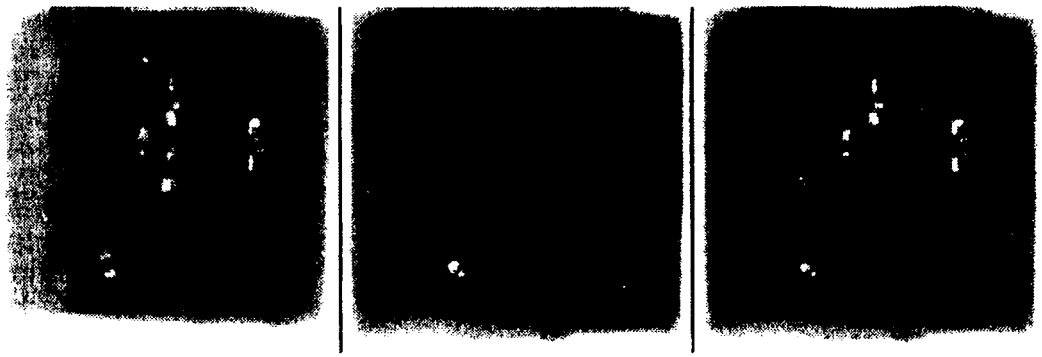

FIGURE 3. Three frames of the same integrated circuit, showing infrared emissions from the device. The pattern of emissions can be used to verify proper operation or to provide valuable clues for diagnosing problems.

4. CONCLUSIONS

We have shown that the quantum efficiency of the high-resistivity CCD is very stable as the temperature of the device is reduced to the typical operating temperature of -120°C. This QE stability should relax the temperature stability requirements for operation of these devices in astronomical instruments and may eliminate the need for an active temperature control system.

We have developed a new clocking scheme that allows us to measure CTE, and we have measured CTE in the serial register of the high-resistivity CCD as high as 0.999999. For one region of the serial register we have measured CTE as a function of signal level. This is a measurement that can't be done with the typical x-ray illumination method because the x-ray method produces a single-size charge packet for each absorbed x-ray.

We have demonstrated an industrial imaging application of the high-resistivity CCD. The application, imaging of the infrared light emissions from an integrated circuit, takes advantage of the CCD's high QE in the near infrared. Compared to a camera equipped with a standard scientific CCD, the high-resistivity CCD camera is at least 40 times faster, making it suitable for real-time monitoring.

ACKNOWLEDGEMENTS

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Fully Depleted, Back-Illuminated Charge-Coupled Devices Fabricated on High-Resistivity Silicon

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***Abstract*—Charge-coupled devices (CCDs) have been fabricated on high-resistivity, n-type silicon. The resistivity, on the order of 10 000 Ω · cm, allows for depletion depths of several hundred micrometers. Fully depleted, back-illuminated operation is achieved by the application of a bias voltage to an ohmic contact on the wafer back side consisting of a thin *in situ* doped polycrystalline silicon layer capped by indium tin oxide and silicon dioxide. This thin contact allows for a good short-wavelength response, while the relatively large depleted thickness results in a good near-infrared response.**

***Index Terms*—Back illuminated, charge-coupled device (CCD), fully depleted, high-resistivity silicon.**

I. Introduction

THE large focal planes of astronomical telescopes require high-quantum-efficiency (QE), large-format charge-coupled device (CCD) detectors. In order to achieve high QE, the standard scientific CCD is thinned and back illuminated [1]. Thinning is required because the relatively low-resistivity silicon used to fabricate scientific CCDs limits the depth of the depletion region. In order to minimize field-free regions with resulting degradation in spatial resolution, the typical scientific CCD is thinned to about 20 μm. This process degrades red and near-infrared responses due to the rapid increase in absorption length in silicon at long wavelengths. In addition, fringing patterns due to multiply-reflected light are observed in uniformly illuminated images taken at near-infrared wavelengths where the absorption length exceeds the CCD thickness. The CCD described in this work achieves high QE in the red and near-infrared by virtue of a thick depleted region made possible by the use of high-resistivity silicon substrates.

Extended red response is extremely important to the Supernovae Cosmology Project at Lawrence Berkeley National Laboratory (LBNL) due to the use of distant, high redshift supernovae for the determination of cosmological parameters [2]. Detection and follow-up spectroscopy of high redshift objects would greatly benefit from CCDs with improved near-infrared response.

We have reported results on a small prototype CCD with high QE extended to 1000 nm [3], [4]. In this work, the physical operating principles and technology of this CCD are described along with results on large-format sensors.

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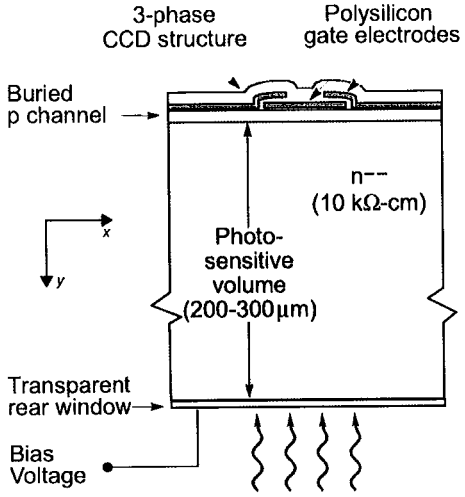

Fig. 1. Cross-sectional diagram of the CCD described in this work. The actual implementation of the substrate bias voltage connection is described in Section III.

II. Background

Scientific CCDs are typically used in applications requiring low level light detection. Hence dark current, noise, and QE are of primary importance. For astronomy applications the CCDs are often cooled to −120 °C to −150 °C to minimize dark current. In addition, readout rates are relatively slow, typically 20–50 kpixels/s, to minimize read noise [1]. The signal-to-noise ratio (SNR) is further increased by the use of back illumination with correspondingly high QE. Large-format sensors are commonly used, and high charge transfer efficiency (CTE) is required.

Fig. 1 shows a cross section of the CCD considered in this work. A conventional three-phase, triple polysilicon gate CCD [5] with buried channel is fabricated on a high-resistivity n-type substrate. A substrate bias is applied to fully deplete the substrate, which is typically 200–300 μm thick. The biasing details are described in Section III. The CCDs described in this work are fabricated on 10 000–12 000 Ω · cm material, corresponding to a donor density N_D of approximately 3.6–4.3 × 10^{11}cm^{-3}. This high-resistivity starting material allows for fully depleted operation at reasonable voltages.

The CCD described here is p-channel. The choice of p-channel over the more conventional n-channel was due to our previous experience with fabrication of charged-particle p–i–n

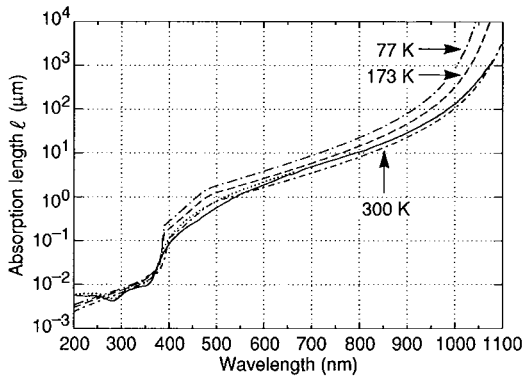

Fig. 2. Absorption length versus wavelength for silicon. Data and calculations (dashed lines) are taken from [18]. Additional room-temperature data (solid line) are taken from [1].

detectors, where we found it more straightforward to produce low dark current devices via backside gettering techniques on n-type silicon [6]. The degraded readout speed resulting from lower hole mobility in a p-channel CCD is not a concern for the astronomy application due to the relatively low readout rates. P-channel CCDs are presently under study for space applications due to the expected improvement in resistance to damage produced by high-energy protons in the space environment when compared to n-channel CCDs [7]–[9].

Previous n-channel "deep-depletion CCDs" [10]–[14] have 40–80-μm-thick depletion regions, due to the use of more highly doped starting silicon and the lack of a substrate bias voltage. Early work on CCDs fabricated on high-resistivity n-type silicon was reported, although problems with high dark current were noted [15], [16]. The same group later described fully depleted, deep-depletion n-channel CCDs with implanted backside layers [17]. In the prior work cited, the interest was primarily in extended X-ray response. As noted earlier, our interest in a thick CCD is motivated by improved near-infrared response. Fig. 2 shows calculated absorption length in silicon as a function of wavelength [18]. Absorption length is defined here as the reciprocal of absorption coefficient α defined in terms of attenuation of incident light intensity I_0 with depth y, i.e., $I(y) = I_0 e^{-\alpha y}$.

Given that silicon is an indirect-gap semiconductor, two regions are of interest. For photon energies above the direct bandgap energy of 2.5 eV, corresponding to a wavelength of approximately 500 nm, light absorption is highly efficient and the absorption coefficient is determined by available conduction band states [19], [20]. Hence, the absorption coefficient for direct transitions α_d varies as the square root of energy as per the energy dependence of the conduction band density of states, i.e.,

$$\alpha_d = A\sqrt{h\nu - E_{g,\mathrm{direct}}(T)}. \tag{1}$$

The temperature dependence is due to the bandgap term $E_{g,\mathrm{direct}}(T)$ and is relatively weak in the direct gap regime. A is a constant, $h\nu$ is the photon energy, and T is the absolute temperature.

Below photon energies of 2.5 eV, phonons are required for momentum conservation and the absorption process becomes less efficient and more sensitive to temperature due to the phonon statistics. In the indirect absorption regime, the absorption coefficient goes as [19], [20]

$$\alpha_i = \frac{B(h\nu - E_{g,\mathrm{indirect}} + E_p)^2}{\exp\left(\frac{E_p}{kT}\right) - 1} + \frac{B(h\nu - E_{g,\mathrm{indirect}} - E_p)^2}{1 - \exp\left(\frac{-E_p}{kT}\right)} \tag{2}$$

where the terms are due to phonon absorption and emission, respectively. k is Boltzmann's constant, E_p is the phonon energy, and B is a constant. Equation (2) is valid for photon energies greater than $E_{g,\mathrm{indirect}} + E_p$ while only the phonon absorption term contributes to the absorption coefficient for photon energies of $E_{g,\mathrm{indirect}} \pm E_p$.

The net result is an absorption length that increases with wavelength as shown in Fig. 2. At photon energies comparable to the indirect bandgap energy, the absorption length can be more than 100 μm, requiring thick CCDs to achieve high QE in the near-infrared.

An advantage of a thick CCD fabricated on high-resistivity silicon is that the CCD clock levels can be set to optimize performance parameters such as charge transfer efficiency and well depth while the nearly independent substrate bias is used to achieve full depletion. A one-dimensional (1-D) depletion-approximation solution to the Poisson equation for a thick CCD with applied substrate bias is given in Appendix A. The potential V_J at the buried-channel/substrate junction is approximately equal to the potential minimum $V_{\min}$ and is given by

$$V_J \approx V_G - V_{\mathrm{FB}} - \frac{qN_A}{2\epsilon_{\mathrm{Si}}} {y_J}^2 \left(1 + \frac{2\epsilon_{\mathrm{Si}} d}{\epsilon_{\mathrm{SiO_2}} y_J}\right) \tag{3}$$

which is independent of the substrate bias voltage V_{sub}. V_G is the applied gate voltage, V_{FB} is the flat-band voltage, q is the electron charge, N_A is the doping density in the p channel of depth y_J, d is the gate insulator thickness, and ϵ_{Si} and $\epsilon_{\mathrm{SiO_2}}$ are the permittivities of silicon and silicon dioxide, respectively.

This approximation is valid for $N_D \ll N_A$ and $y_N \gg y_J + (\epsilon_{\mathrm{Si}}/\epsilon_{\mathrm{SiO_2}})d$, where y_N is the thickness of the fully depleted, n-type region with doping density N_D (see App. A, Fig. 16). For the CCDs considered here, N_D is more than four orders of magnitude less than N_A, and therefore only a small fraction of the field lines from the channel are required to terminate in the substrate. Hence, nearly all the field lines from the channel terminate in the gate, which is the physical interpretation of (3). The third and fourth terms of (3) are the voltage drops across the fully depleted channel and the voltage drop across the oxide when the channel is fully depleted. Equation (3) is a 1-D approximation to a decidedly two-dimensional (2-D) problem, and it is shown in Appendix A that the effect of the barrier phases is to slightly raise the value of V_J when compared to the 1-D approximation. However, it is still true that the potential at the junction is a weak function of the substrate bias due to the large difference in doping between the channel and substrate and the use of a thick depleted substrate.

In addition, a thick CCD reduces fringing [21]. In thinned CCDs, fringing arises due to multiple reflections at long wavelengths when the absorption length of the incident light is greater than the CCD thickness. Fringing as well as the

loss of QE limits the usefulness of scientific CCDs at long wavelengths.

There are several drawbacks to a thick CCD, however. Charged-particle events from cosmic rays and terrestrial radiation sources will affect more pixels in a thick CCD [22]. Also, a larger volume for near-infrared response implies more volume for dark current generation and care must be taken during processing to minimize dark current. In addition, reduction of surface current due to interface states is not as straightforward as in a thinned CCD with no substrate bias, although, as shown later, surface dark current suppression can be done satisfactorily at cryogenic temperatures.

In low-f number optical systems where the light is incident at large angles from the normal, there will be depth-of-focus issues for long-wavelength light absorbed at significant depths, although the large refractive index of silicon helps in this regard by "straightening" the light. At the short-wavelength end, the photogenerated holes must traverse nearly the entire thickness of the CCD, and spatial resolution is a concern. This is discussed in more detail in Section VI. In Section III, the fabrication technology is described, followed by discussion of transistor behavior of buried channel MOS devices fabricated on high-resistivity silicon.

III. CCD Fabrication and Back-Illumination Technology

The CCDs discussed in this work were fabricated at the LBNL Microsystems Laboratory [3]. The starting material was 100-mm-diameter, (100), high-resistivity, n-type silicon manufactured by Wacker Siltronic.

The gate insulator consists of 500 Å of thermally grown SiO_2 and 500 Å of low-pressure chemical vapor deposited (LPCVD) Si_3N_4. The triple polysilicon gate structures are plasma etched in Cl_2/HBr for high selectivity to the underlying Si_3N_4 layer. Single-level Al–Si is used for metallization. *In situ* doped (phosphorus) polysilicon is used for extrinsic gettering [6], and this layer is deposited on the back side of the wafer early in the process and capped with Si_3N_4 to eliminate oxidation of the layer and possible autodoping during subsequent processing. A notch implant [23] is included in the process and is used in the serial register to confine small-signal charge packets to a 3-μm-wide channel in the serial register, which is wider than the vertical channel to accommodate binning.

Fig. 3 shows an example of a 100-mm-diameter wafer fabricated at LBNL. The large devices in the center of the wafer are 2048 × 2048, 15-μm pixel CCDs. The vertical register is split into two equal regions allowing for frame store operation, although in most cases the two sets of vertical clocks are connected and the CCD is operated as a frame transfer device. The serial register located along one side of the CCD is similarly split, allowing for readout to either amplifier or to both for faster readout rates. The wafer also includes additional 15- and 24-μm pixel CCDs.

Since the structure shown in Fig. 1 is essentially a CCD merged with a p–i–n diode, we require a backside ohmic contact in order to apply the substrate bias needed to fully deplete the wafer thickness. This ohmic contact layer must be thin to allow for short-wavelength light transmission. In Fig. 2, it can be seen that the absorption length is less than 0.1 μm for wavelengths less than about 400 nm, and becomes less than 100 Å at ultraviolet (UV) wavelengths.

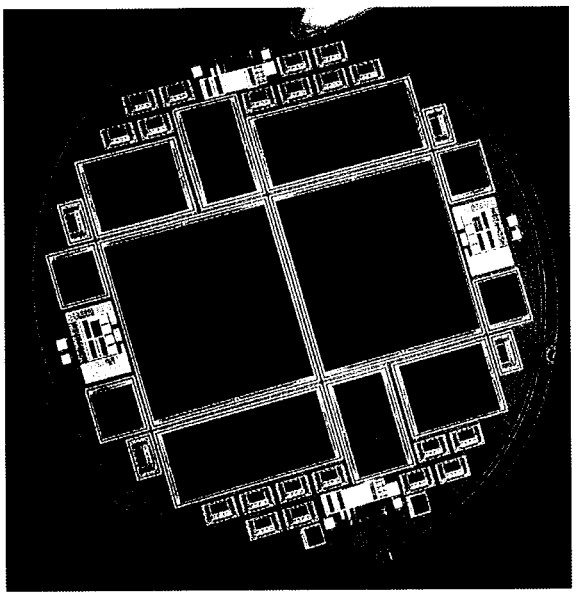

Fig. 3. A 100-mm-diameter wafer fabricated at LBNL. The two large CCDs in the center of the wafer are 2048 × 2048, 15 μm pixel, frame transfer CCDs.

Previous back-illumination techniques for conventional scientific CCDs include UV flooding [24] and laser annealing of an ion-implanted backside layer [13], [25]. In both cases, a built-in field is generated to overcome the native depletion layer at the backside surface for p-type silicon due to positive fixed oxide charge at the silicon–SiO_2 interface [1]. Laser annealing is required since the thinning step is performed on a finished wafer and the annealing temperature of the backside implant is limited to $\approx$ 475–525 °C depending on the metallization used [26].

Since the devices fabricated on high-resistivity silicon can be made relatively thick, it is possible to create the backside layer as a high-temperature step before the Al is deposited. Bosiers *et al.* [17] were able to demonstrate conventional high-temperature annealing of an implanted backside p^+ layer by virtue of the use of relatively thick (150 μm and below) high-resistivity substrates that could be processed through the metallization step after the implant was annealed. Our technique involves removing the $\approx$ 1-μm-thick n^+ polysilicon gettering layer before the contact mask. The wafers are sent to a commercial vendor for backside polishing to the final desired thickness. Polishing of the backside surface is required for an optical quality surface, and in our experience this is especially an issue for long-wavelength light.

After the polishing step, the backside ohmic contact is formed by depositing a thin ($\approx$ 20 nm) layer of *in situ* doped (phosphorus) polysilicon [27]. This layer is deposited by LPCVD at 650 °C using 1.5% PH_3 in SiH_4 as the source gas. A sacrificial oxide is then sputtered on the back side and the wafers are processed through the contact and metal steps. During these steps, the wafers are thinner than standard. We have found that 200–300-μm-thick, 100-mm-diameter wafers can be processed

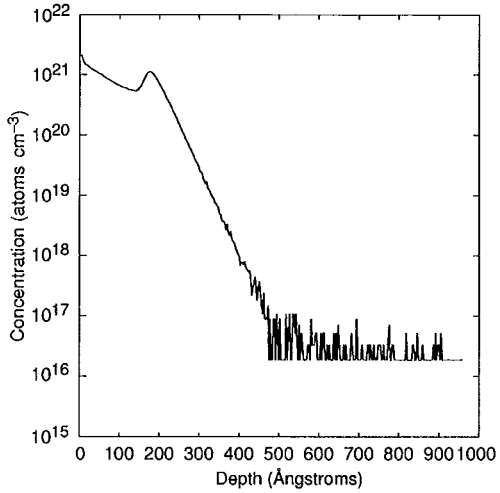

Fig. 4. SIMS depth profile of the thin back-side ohmic contact used in this technology. The layer is fabricated by *in situ* doped (phosphorus) polysilicon deposition. The detection limit for phosphorus was 1×10^{16} cm^{-3}.

with standard processing equipment. This becomes more challenging as one scales to larger diameter wafers. Modification of some automatic wafer handling equipment was required in order to avoid damaging the backside surface, as well as to minimize particle deposition on the back side. In addition, particle removal via scrubbing is used to reduce the final particle count on the back side of the wafer. If this is not done, uniformly illuminated images (flat fields) taken in the UV can show particle patterns from the various wafer handlers used in the process.

Fig. 4 shows a secondary ion mass spectroscopy (SIMS) depth profile of the phosphorus concentration for a nominal 200-Å–thick backside polysilicon film. The detection limit was 1×10^{16} cm^{-3} and the spatial resolution limit was 65 Å/decade. As can be seen in Fig. 4, a very thin layer is possible with this technique. The peak in the phosphorus concentration could be due to phosphorus pile-up at the original polysilicon–silicon interface resulting from perhaps a native oxide layer present at that interface [28]. In general, this is not desirable due to the potential for a built-in field that would oppose hole flow for carriers generated in the polysilicon layer, although poor collection efficiency is expected there because of low minority carrier lifetime due to Auger recombination.

It will be shown later that it is desirable to operate the CCD overdepleted to minimize degradation in spatial resolution. In addition, the fairly large radial variation in resistivity for high-resistivity silicon [29] requires overdepleted operation to guarantee the elimination of field-free regions with correspondingly poor spatial resolution. A possible concern is the effect on dark current for overdepleted operation. Fig. 5 shows measured dark current and inverse square capacitance $1/C^2$ measured on 2-mm^2 p–i–n diode test devices. Results are shown from wafers of thickness $\approx$ 200 and 275 μm. These wafers went through the entire CCD process. The backside polysilicon thickness is $\approx$ 200 Å. The dark current at room temperature is less than 0.2 nA/cm^2 and does not increase significantly for bias voltages above that necessary for full depletion, where the $1/C^2$ curves approach a constant level. Therefore, the gettering

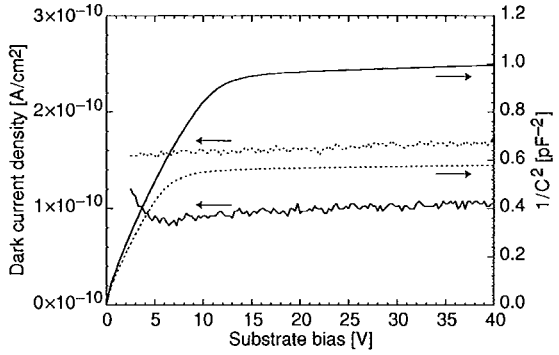

Fig. 5. Inverse square capacitance and reverse leakage current measured at room temperature on 2-mm^2 p–i–n diode test structures from CCD wafers. Data are shown for 200- (dotted lines) and 275-μm–thick (solid lines) wafers.

process is effective in maintaining low dark current for large depletion depths, and the thin polysilicon deposition step does not degrade the dark current.

After the 400 °C sintering step, the back-side sacrificial oxide is removed and $\approx$ 600 Å of indium tin oxide (ITO) is deposited [27]. The ITO functions as part of an antireflection (AR) coating and improves the conductivity of the back side, where an equipotential is desired as described below. A second AR coating of $\approx$ 1000 Å of SiO_2 is added to form a two-layer AR coating optimized for near-IR detection [21]. Fig. 6 shows the measured QE of an $\approx$ 280-μm-thick, 1980 $\times$ 800, 15-μm pixel back-illuminated CCD with the two-layer AR coating. The QE exceeds 90% at near-IR wavelengths and is still $\approx$ 60% at a wavelength of 1 μm. For a detailed discussion of QE modeling results for these CCDs, the reader is referred to [21].

As a practical matter, it is not convenient to make a direct electrical connection to the back side of the wafer as shown in Fig. 1. Doing so would complicate the use of insulating AR coatings, for example. Instead, in the actual implementation, the contact is made on the front side of the CCD. Fig. 7 illustrates the technique used to bias the CCD. Shown in the figure is a 2-D simulation (Medici 4.0.1) of a p–i–n diode structure on a 280-μm–thick high-resistivity, n-type substrate. The substrate doping used in the simulation was 4.0×10^{11} cm^{-3}. For convenience in the simulation, the 35-V bias voltage was applied to the backside ohmic contact. Beyond the depletion edge, the undepleted region is an equipotential at the applied substrate bias as long as the current flow in this region is negligible. In that case one can equivalently place an n^+ contact at the front side of the CCD in the undepleted region with the same result as shown in Fig. 7 and apply the bias voltage more conveniently there. The function of the floating p^+ guard rings is to gradually drop the potential from the undepleted n region to the grounded p^+ guard ring that surrounds the CCD, thereby maintaining low electric fields at the surface [30]–[32].

Photogenerated electrons are directed by the field in the fully depleted substrate to the backside ohmic contact where they flow laterally and are eventually drained through the undepleted substrate to the front-side n^+ contact located in the undepleted region. For low light level applications, the dc voltage drop in the substrate due to the electron photocurrent is negligible. A 1-Mpixel CCD operating at 30 frames/s with a high light level

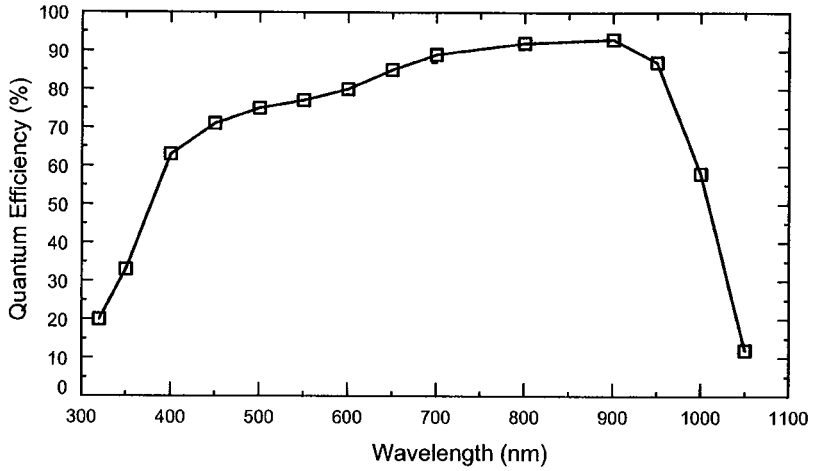

Fig. 6. Quantum efficiency measured on a 1980 × 800, 15-μm pixel back-illuminated, fully depleted CCD. The measurement was performed at Lick Observatory and the operating temperature was −130 °C. The thickness was ≈ 280 μm.

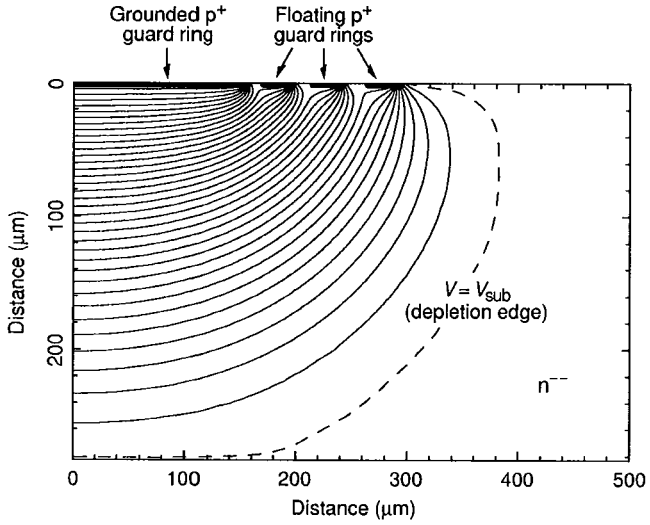

Fig. 7. Two-dimensional simulation of a p–i–n diode structure on high-resistivity silicon. The equipotential lines are spaced at 1-V intervals. The substrate bias voltage was 35 V and the substrate doping and thickness were 4×10^{11} cm^{-3} and 280 μm, respectively.

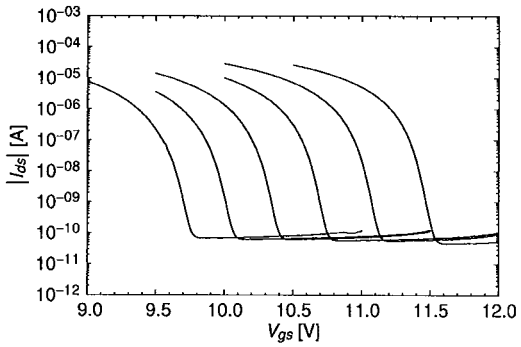

Fig. 8. Measured subthreshold characteristics of a 47/6 buried channel PMOSFET with 1.5-μm gate-to-source/drain spacing. The substrate bias varied from 25 (rightmost curve) to 75 V (leftmost curve) in 10-V steps. The temperature was −128 °C, and the drain to source voltage was −1 V.

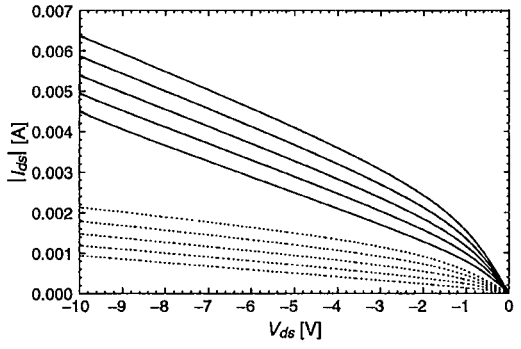

Fig. 9. Room-temperature output characteristics of a 51/2 buried channel PMOSFET with 1.5-μm gate-to-source/drain spacing (lower curves, dotted) compared to a self-aligned transistor (upper curves, solid). The substrate bias was 25 V. The gate voltage was varied from 7.5 to 3.5 V in 1-V steps.

corresponding to 100 ke$^-$/pixel would have an electron photocurrent of only ≈ 0.5 μA, for example, while in low level light applications the photocurrent would be orders of magnitude smaller. The dc voltage drop in the backside ohmic contact resulting from a lateral drift of electrons along the backside contact is minimized by the use of the ITO AR layer that has a typical sheet resistance of 40 Ω/square. This biasing scheme was used in all the results presented in this paper.

IV. Transistor Performance

The CCDs described in this work have conventional floating diffusion amplifiers, and p-channel MOSFETs are used for reset and amplification. Given the relatively slow readout rates, the output source follower is buried channel to minimize $1/f$ noise [33], as is the reset transistor. For process simplicity, the transistors are fabricated directly in the high-resistivity substrate without the use of a well. We have found such transistors to give acceptable performance although future applications could require improvements in transistor characteristics. Several examples of active devices fabricated directly on high-resistivity silicon for high-energy physics applications have been reported [34]–[36], as well as early work on MOS transistors fabricated on high-resistivity silicon [37], [38].

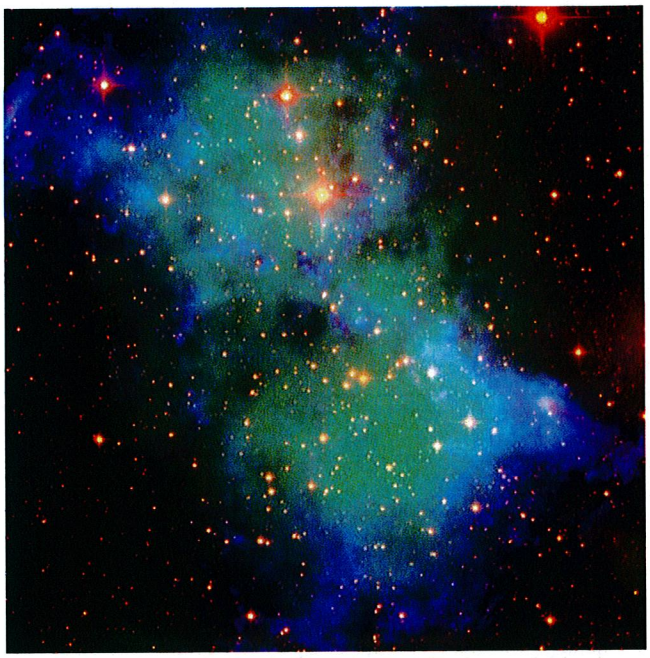

Fig. 10. Far-red/near-infrared image of M27 (Dumbbell Nebula) taken with a fully depleted, back-illuminated 2048 × 2048, 15-μm pixel, high-resistivity CCD. The image was generated from exposures taken at three wavelengths (see text) at the National Optical Astronomy Observatory WIYN 3.5-m telescope.

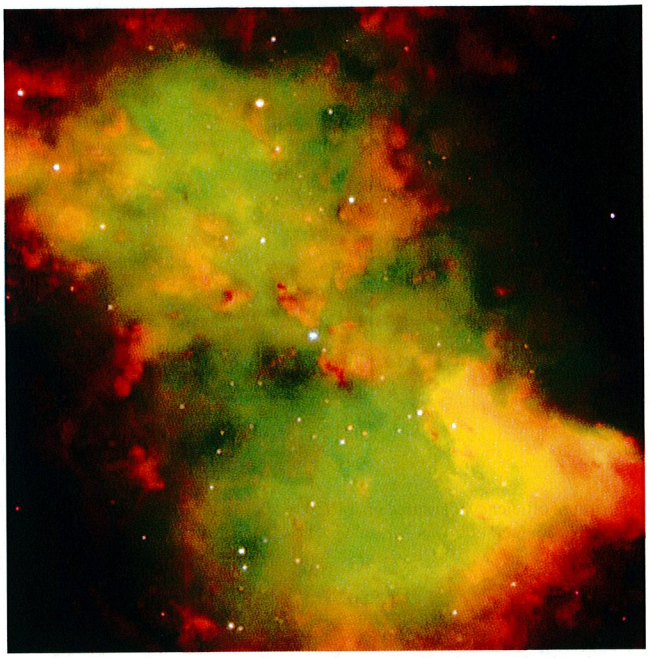

Fig. 11. Visible light image of M27 (Dumbbell Nebula) taken with a commercially available, back-illuminated 2048 × 2048, 24-μm pixel CCD. The image was generated from exposures taken at three wavelengths (see text) at the European Southern Observatory 8.2-m VLT.

The use of extremely low substrate doping in an MOS transistor leads to desirable features such as small bulk-junction capacitance and body effect, as well as undesirable features such as punchthrough and drain-induced barrier lowering. The latter two effects can be reduced somewhat by the application of the substrate bias used to fully deplete the substrate [3], [35]. In addition, the heavily doped source and drain regions can be offset from the gate to improve punchthrough characteristics [39], [40] as well as minimize overlap capacitance [10].

The small body effect realized for these transistors is demonstrated in Fig. 8, which shows subthreshold characteristics measured on a 47/6 MOSFET with 1.5-μm gate-to-source/drain spacing at a temperature of -128 °C for substrate bias voltages ranging from 25 to 75 V. Over this 50-V range in substrate bias, the threshold voltage of the transistor is changed by only $\approx$ 1.8 V, which can easily be accommodated in the CCD biasing. The data of Fig. 8 were measured on a CCD with access to the gate electrode through the reset transistor. The 47/6 transistor is presently used for most single-stage, source-follower amplifier designs in this technology. The CCD was mounted in a commercially available cryogenic dewar. The high off-state leakage current is an artifact of the measurement, and is due to leakage current in the dewar wiring. This device had a boron channel implant dose of 1.3×10^{12} cm^{-2}. The measured subthreshold slope at -128 °C is 50–56 mV/decade.

The effectiveness of a 1.5-μm source-drain-to-gate offset in improving the transistor characteristics is shown in Fig. 9. Output characteristics of transistors with 2-μm channel length are shown. The self-aligned transistor has a significant threshold voltage change as well as higher output conductance when compared to the device with the 1.5-μm gap between the gate edge and heavily doped source and drain.

Hence, the transistor characteristics are adequate for scientific CCD applications even for devices fabricated on 10 000–12 000 $\Omega \cdot$ cm silicon. In Section V, we present data on CCD performance.

V. CCD Performance

Fig. 10[1] shows a far-red/near-infrared image of the Dumbbell Nebula M27 taken at the National Optical Astronomy Observatory WIYN 3.5–m telescope with a back-illuminated 2048 × 2048, 15 μm pixel CCD of the type shown in Fig. 3. This is a false color image taken from exposures with three different filters; a narrow-band filter at the H-α line (6560 Å, blue in the image), a narrow-band filter at the [SIII] line (9532 Å, green in the image), and an intermediate band filter that detects HeII emission (1.0124 μm, red in the image).

For comparison, a visible light image taken at the European Southern Observatory 8.2–m Very Large Telescope (VLT) is shown in Fig. 11.[2] This image was taken with a commercially available, back-illuminated 2048 × 2048, 24-μm pixel CCD. The image is also generated from three filters, although in this case the filters are all in the visible range; a narrow-band filter centered at the [OIII] emission line (5010 Å, green in the image), a narrow-band filter centered at the H-α emission line (6560 Å, red in the image), and a broad-band filter centered at 4290 Å (blue in the image).

The H-α detail is shown nicely in both images. The main difference in the images is the detection of background stars

[1]Image courtesy of N. Sharp, R. Reed, D. Dryden, D. Mills, D. Williams, C. Corson, R. Lynds, and A. Dey, National Optical Astronomy Observatory, WIYN Observatory, and National Science Foundation.

[2]Image courtesy of the European Southern Observatory.

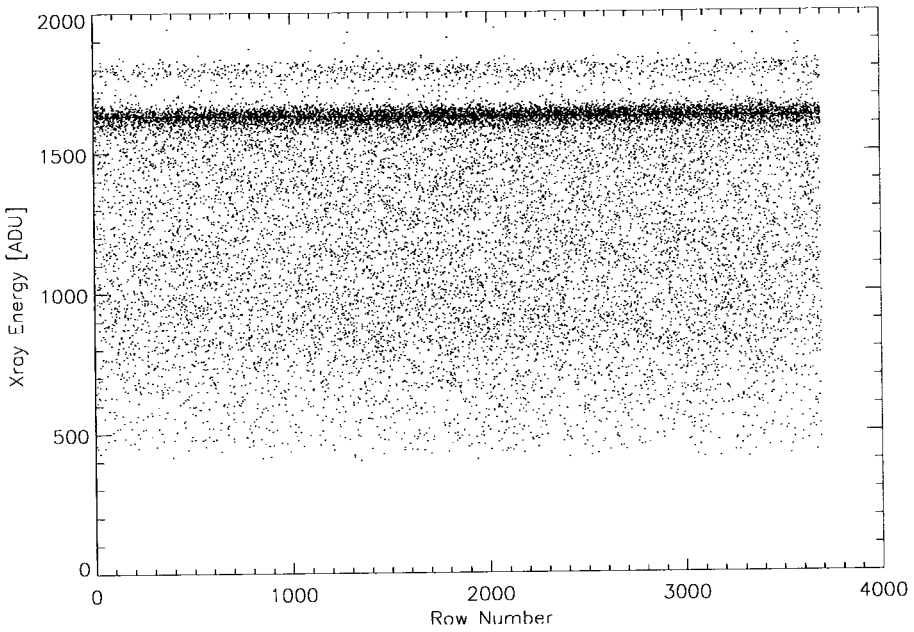

Fig. 12. Vertical charge transfer efficiency measured at −130 °C on a 1478 × 4784, 10.5-μm pixel CCD.

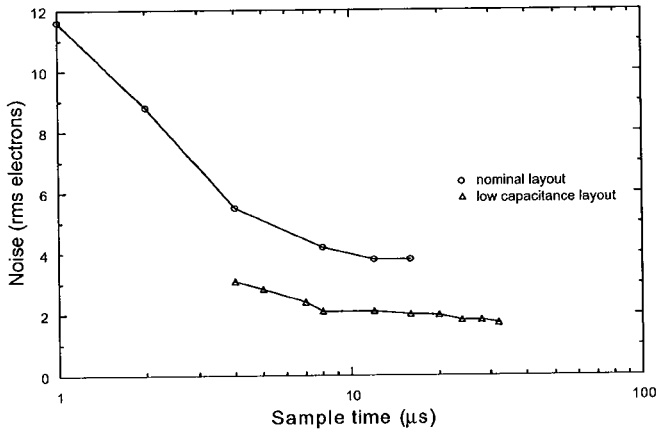

Fig. 13. Noise after double-correlated sampling versus sample time at −130 °C comparing 47/6 output transistors with varying size metal interconnects between the floating diffusion and output transistor.

in the 1.0124-μm exposure, which are not seen in the image of Fig. 11 due to absorption of the visible wavelengths of the background light in the dust and gas in the vicinity of the nebula. Imaging at $\approx$ 1 μm with high QE and negligible fringing is a unique feature of a fully depleted, thick CCD.

Figs. 12 and 13 show CTE and noise results. CTE was measured with an ^{55}Fe source [1] on a front-illuminated, 1478 × 4784, 10.5-μm pixel CCD. In this method, the CCD is exposed to an ^{55}Fe radioactive source that emits K_α and K_β manganese X-rays at energies of 5.9 and 6.5 keV, respectively. The X-rays deposit a well-defined amount of energy in the silicon, which on average is converted to 1620/1778 e^-, respectively, for the K_α/K_β X-rays. In Fig. 12, each column of the CCD is read out in analog to digital units (ADUs), and all columns are stacked together in a single plot. The dark band is the cluster of K_α events and is used for both CTE determination and amplifier calibration. Events below this dark band are X-ray events where the charge was split into multiple pixels. The faint band above the K_α single-pixel events is the K_β band. The slope of the K_α band gives a global measure of CTE. Devices with poor CTE will show decreasing X-ray counts with increasing charge transfer distance (row number in Fig. 12) or, stated differently, a negative slope on a plot such as shown in Fig. 12. The measurement is global in the sense that information regarding the column number of the X-ray event is not displayed in such a plot. Related to this, the serial CTE must be good in order to not affect the vertical CTE measurement. Serial CTE is determined in a similar fashion, with ADU counts plotted against column number. We typically observe no significant difference between serial and vertical CTE. The CTE defined in terms of pixel transfers determined from the data of Fig. 12 was 0.999 998 7 at −130 °C, and CTEs exceeding 0.999 995 are typical for devices fabricated on high-resistivity silicon at LBNL. The data were truncated at $\approx$ 3700 rows due to decreasing X-ray counts resulting from the finite size of the X-ray source. Nonetheless, 3700 rows corresponds to a transfer length of $\approx$ 4 cm, and a CTE of 0.999 998 7 corresponds to less than 1% loss in signal after 4784 vertical charge transfers.

The read noise was previously reported to be 4–6 electrons [4] and has been improved to as low as $\approx$ 2 electrons by reducing the parasitic capacitance at the floating diffusion, as seen in Fig. 13. Minimization of the area of the aluminum trace from the floating diffusion to the gate of the output 47/6 MOSFET accounts for most of the improvement noted in Fig. 13. Charge-to-voltage conversion factors are estimated to be 2.0 and 3.5 μV/e$^-$ for the old and new amplifiers, respectively. Even lower noise has been reported with the use of a buried contact technology to minimize the interconnect capacitance [13].

Dark currents of a few electrons per pixel per hour have been achieved at low temperatures. The importance of gettering to

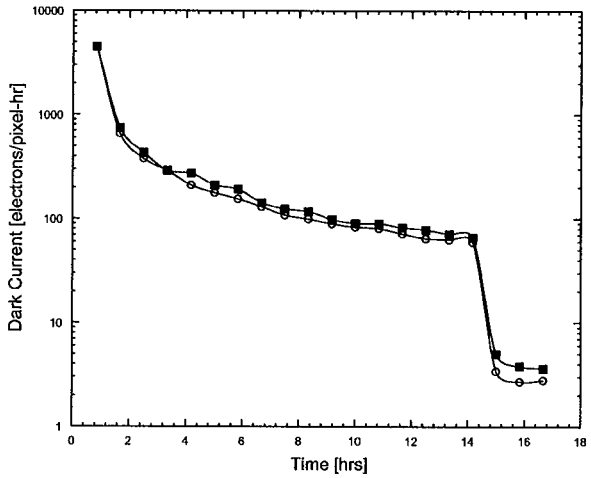

Fig. 14. Dark current versus time measured at −150 °C for a back-illuminated, 2048 × 2048 CCD. At time zero the CCD is overexposed to light, resulting in a residual image that detraps with a long time constant at −150 °C. After 14 h, the "erase" cycle described in the text is employed to erase the residual image and reduce the surface dark current by trapping electrons in the interface states. The open symbols are for dark current measured near the serial register, and the closed symbols are for measurements far from the serial register.

achieve low dark current was previously described. Surface dark current arising from surface states at the silicon–silicon dioxide interface is also an important issue [41]. In typical scientific CCDs, the surface dark current is reduced by operating the surface of the buried channel in inversion at least part of the clock cycle [42]–[44].

A supply of inversion layer carriers from the implanted channel stops located between channels is not straightforward when relatively large substrate bias voltages are applied, as in the case of the CCDs considered in this work. This is a drawback to the use of a substrate bias to fully deplete the CCD. Nonetheless, one can take advantage of the temperature dependence of the time constant for detrapping of charges trapped in interface states [45]. At the low operating temperatures considered here, the time constants are on the order of hours. Fig. 14 shows experimental data taken at −150 °C on a back-illuminated, 2048 × 2048 CCD. The CCD was exposed to a light level exceeding the full-well capacity, resulting in photogenerated holes trapped at interface states. This charge gradually detraps during subsequent frames, causing a residual image [1]. After 14 h, the CCD then goes through an "erase" cycle that consists of lowering the substrate bias to 0 V and increasing the positive vertical clock levels to a value sufficient to invert the surface with electrons from the channel stops. After the erase cycle, the CCD is operated with the normal substrate bias voltage and more dark frames are taken. The erase cycle fills the interface states with electrons, and, as shown in Fig. 14, dark currents on the order of a few electrons per pixel per hour are then achieved at the cryogenic operating temperatures of interest for the astronomy application.

VI. Spatial Resolution

A concern for the fully depleted, back-illuminated CCD is spatial resolution degradation resulting from lateral spreading via diffusion of the photogenerated charge during the transit from the back side of the device, where short-wavelength light is absorbed, to the CCD potential wells located as far as 300 μm away. We first analyze the charge spreading for the case of a fully depleted p–i–n diode. The charge spreading is described by the point spread function (PSF), which is the impulse response of the optical system [46]. It can be shown that, for carriers arriving at the potential wells at the same time, the solution to the continuity equation for the lateral charge spreading is Gaussian [47]. The charge spreading is characterized by a standard deviation σ given by $\sqrt{2Dt_{\rm tr}}$ where D is the diffusion coefficient and $t_{\rm tr}$ is the carrier transit time [48]. Assuming the fields are below the velocity saturation limit, the drift velocity of the holes is given by

$$v_{\rm DRIFT} = \frac{dy}{dt} = \mu_p E(y) = \mu_p \left(E_{\rm max} + \frac{\rho_n}{\epsilon_{\rm Si}} y \right) \quad (4)$$

where $E(y)$ is the electric field and μ_p is the hole mobility. The expression for $E(y)$ given above is for the case of a simple p^+-n^--n^+ structure that is overdepleted. $\rho_n = q\,N_D$ is the volume charge density in the depleted region. $E_{\rm max}$ is the field at the p–n junction and is given by

$$E_{\rm max} = -\left(\frac{V_{\rm appl}}{y_D} + \frac{1}{2}\frac{\rho_n}{\epsilon_{\rm Si}} y_D \right) \quad (5)$$

where $V_{\rm appl}$ is the voltage drop across the drift region and is assumed to be larger than the depletion voltage $\rho_n {y_D}^2/(2\epsilon_{\rm Si})$. The origin is taken at the p-n junction where $E = E_{\rm max}$, and the n^+ region begins at y_D, i.e., y_D is the thickness of the depleted region and $E(y_D) = E_D$.

Solving (4) and making use of the Einstein relation $D/\mu_p = kT/q$ yields

$$\sigma_{\rm od} = \sqrt{2Dt_{\rm tr}} = \sqrt{2\frac{kT}{q}\frac{\epsilon_{\rm Si}}{\rho_n} \ln \frac{E_{\rm max}}{E_D}}. \quad (6)$$

The subscript indicates that this result is for an overdepleted region. An implicit assumption used in deriving (6) is that the photons are absorbed at y_D, which is the worst case. At high fields $\sigma_{\rm od}$ approaches the constant-field result

$$\sigma_{\rm od} \approx \sqrt{2\frac{kT}{q}\frac{{y_D}^2}{V_{\rm appl}}} \quad (7)$$

which is independent of N_D, directly proportional to y_D, and proportional to $\sqrt{T}$ and $1/\sqrt{V_{\rm appl}}$. While the above derivation is for a simple p^+-n^--n^+ structure, the results are also applicable to a fully depleted CCD. The field at the p–n junction of an overdepleted CCD is given by (see Appendix A)

$$E_J \equiv -\frac{dV}{dy}(y_J) = -\left(\frac{V_{\rm sub} - V_J}{y_N} + \frac{1}{2}\frac{\rho_n}{\epsilon_{\rm Si}} y_N \right) \quad (8)$$

which is of the same form as (5). V_J is the potential at the buried channel junction located at y_J, $V_{\rm sub}$ is the substrate bias voltage, and y_N is the thickness of the lightly doped, fully depleted region. V_J was given earlier in (3). From these equations, the maximum field in the drift region depends on both applied voltages (V_G and $V_{\rm sub}$) and the channel implant dose $N_A y_J$.

Equations (3) and (8) are derived from a 1-D analysis. For CCDs on high-resistivity silicon, the potentials are strongly 2-D [11], [15], since a region exists below the buried channel implant where the field is significantly larger than predicted by (8). As a practical matter, the charge spreading in the high-field region is negligible and (8) can still be used, but V_J is not the potential at the junction but an average potential where the field deviates from (8).

We next derive the PSF for conventional back-illuminated scientific CCDs that typically have a region of zero electric field between the back side illumination surface and the CCD potential wells [1], [49]. The modulation transfer function (MTF) was theoretically analyzed for this case by Crowell and Labuda [50], where MTF is the magnitude of the Fourier transform of the PSF [46]. This work was later extended by Seib [51] to include the possibility of multiple reflections as would occur when the absorption depth of the incident light is larger than the thickness of the device. Details are given in Appendix B, where it is shown that for negligible recombination and light absorbed near the back surface such that the absorption depth is small compared to the field-free thickness, the MTF is given by

$$\mathrm{MTF}_{\mathrm{ff}} \approx \frac{1}{\cosh(kL_{\mathrm{ff}})} \tag{9}$$

where $k = 2\pi f$ where f is the spatial frequency and L_{ff} is the field-free thickness. The PSF is the inverse Fourier transform of the MTF and is then

$$\mathrm{PSF}_{\mathrm{ff}} = \frac{1}{2L_{\mathrm{ff}} \cosh\left(\dfrac{\pi x}{2L_{\mathrm{ff}}}\right)} \tag{10}$$

where x is the lateral dimension (see Fig. 1). The rms standard deviation can be calculated from the Moment Theorem [52] and is given by

$$\sigma^2 = \frac{-F^{(2)}(0)}{4\pi^2 F(0)} + \frac{1}{4\pi^2}\left[\frac{F^{(1)}(0)}{F(0)}\right]^2 \tag{11}$$

where $F^{(n)}(0)$ is the nth derivative of the Fourier transform F evaluated at the origin. Substitution of (9) with $k = 2\pi f$ into the above yields the simple result

$$\sigma_{\mathrm{ff}} = L_{\mathrm{ff}} \tag{12}$$

and hence the rms standard deviation for the field-free case is just equal to the field-free thickness. This result was previously given based on the results of Monte Carlo simulations [53]. The above analysis is highly simplified and is not rigorously valid given the fact that CCDs do not meet the shift-invariance requirement for the use of Fourier transforms in the modeling of MTF and PSF [46], [52].

Nonetheless, it is informative to compare the rms standard deviations of charge spreading for the case of an overdepleted substrate (7) and where the field-free thickness dominates (12). Calculations of CCD depletion depth using the equations in Appendix A for a conventional CCD with no applied substrate bias show that the depletion depth is on the order of ≈ 8 μm for a substrate resistivity of 20 $\Omega \cdot$ cm at a gate voltage of 10 V with a uniform channel doping of 2×10^{16} cm^{-3}. Hence, a typical 20-μm-thick back-illuminated CCD fabricated on 20-$\Omega \cdot$cm silicon with no substrate bias could have a σ of about 12 μm. This can be improved with further thinning but at the expense of red response and fringing.

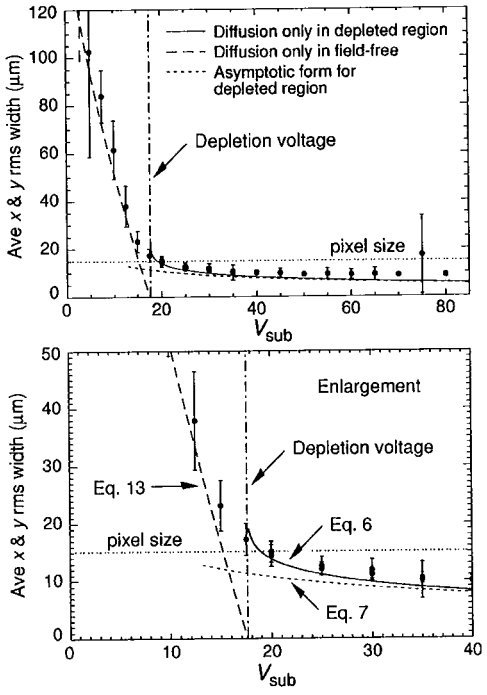

Fig. 15. Measured charge spreading σ using a pinhole mask placed directly on the backside of a back-illuminated CCD fabricated on high-resistivity silicon.

In the overdepleted case, the lateral diffusion can be reduced by lowering the thickness and/or operating temperature and by increasing the substrate bias. Fig. 15 shows experimental data of charge spreading versus substrate bias voltage for an $\approx$ 300-μm-thick CCD at -130 °C. The charge spreading was measured by illuminating the CCD through a chrome-on-quartz pinhole mask that was placed directly on the back surface of the CCD. In order to maximize the transit distance of the photogenerated holes, 400-nm light was used.

At a typical substrate bias voltage of 40 V, σ is about 8–10 μm, which would be comparable to the theoretical calculation given above for a conventional back-illuminated CCD fabricated on 20-$\Omega \cdot$ cm silicon. Therefore, even though the CCD fabricated on high-resistivity silicon is much thicker than its low-resistivity counterpart, the spatial resolution can be comparable and in some cases better. Measurements at the Lick Observatory Hamilton Spectrograph on a 200-μm-thick, 2048 $\times$ 2048, 15-μm pixel CCD give an overall PSF of $\approx$ 1.4 pixels full-width at half-maximum (FWHM), compared to a value of $\approx$ 2.1 pixels FWHM measured on a thinned, back-illuminated CCD [54].

Fig. 15 also includes theoretical curves for the charge spreading. Two parameters, the doping density N_D and potential at the buried channel junction V_J, are required for the theoretical curves shown in the figure [see (3) and (6)–(8)]. These are determined from data taken below full depletion where the field-free thickness dominates the σ measurement

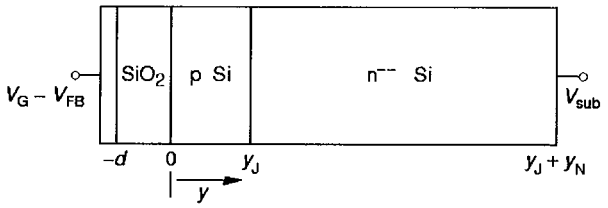

Fig. 16. CCD cross section.

and where the field-free thickness varies with N_D and V_J as per simple p–n junction theory [55], i.e.,

$$L_{\text{ff}} = y_N - \sqrt{\frac{2\epsilon_{\text{Si}}}{qN_D}(V_{\text{sub}} - V_J)} \tag{13}$$

A plot of $(y_N - L_{\text{ff}})^2$ versus V_{sub} should yield a straight line from which N_D and V_J can be determined.

VII. Summary

Fully-depleted CCDs fabricated on high-resistivity silicon have been shown to have improved characteristics at near-infrared wavelengths when compared to conventional scientific CCDs. Physical operating principles of the fully depleted CCD have been presented along with technology issues and performance results. Tradeoffs in terms of QE and spatial resolution as determined by device thickness and operating temperature can be analyzed based on the results given in this work and optimized for a given application.

Appendix A
Derivation of Potentials and Fields for an Overdepleted CCD

Fig. 16 shows the cross section of the CCD. The origin is taken at the silicon–SiO_2 interface. The gate insulator thickness is d, the junction depth is at y_J, and the thickness of the substrate is $y_J + y_N$. We treat the junction at the substrate—n^+ backside ohmic contact (not shown) as a one-sided step junction and neglect the voltage drop in the backside ohmic contact. The CCD is assumed to be overdepleted in what follows.

Poisson's equation in the various regions is

$$\frac{d^2V}{dy^2} = 0, \quad -d < y < 0 \tag{A1}$$

$$\frac{d^2V}{dy^2} = \frac{qN_A}{\epsilon_{\text{Si}}}, \quad 0 < y < y_J \tag{A2}$$

$$\frac{d^2V}{dy^2} = \frac{-qN_D}{\epsilon_{\text{Si}}}, \quad y_J < y < (y_J + y_N). \tag{A3}$$

The solutions to Poisson's equation subject to the boundary conditions $V(-d) = V_G - V_{\text{FB}}$, $V(y_J + y_N) = V_{\text{sub}}$, and continuity of electric field and potential at $y = 0$ and y_J are

$$V(y) = V_G - V_{\text{FB}} - E_{\text{SiO}_2}(y + d), \quad -d < y < 0 \tag{A4}$$

$$V(y) = V_{\min} + \frac{qN_A}{2\epsilon_{\text{Si}}}(y - y_{\min})^2, \quad 0 < y < y_J \tag{A5}$$

$$V(y) = V_J - \frac{qN_D}{2\epsilon_{\text{Si}}}(y - y_J)^2 - E_J(y - y_J), \quad y_J < y < (y_J + y_N) \tag{A6}$$

where $V_J \equiv V(y_J)$, $V_{\min} \equiv V(y_{\min})$, i.e., $y_{\min}$ is the location of the potential minimum. The corresponding electric fields are

$$E(y) = E_{\text{SiO}_2}, \quad -d < y < 0 \tag{A7}$$

$$E(y) = -\frac{qN_A}{\epsilon_{\text{Si}}}(y - y_{\min}), \quad 0 < y < y_J \tag{A8}$$

$$E(y) = \frac{qN_D}{\epsilon_{\text{Si}}}(y - y_J) + E_J, \quad y_J < y < (y_J + y_N). \tag{A9}$$

The electric fields are defined by

$$E_{\text{SiO}_2} \equiv -\frac{dV}{dy}(0^-) \tag{A10}$$

$$E_J \equiv -\frac{dV}{dy}(y_J) = -\left(\frac{V_{\text{sub}} - V_J}{y_N} + \frac{1}{2}\frac{qN_D}{\epsilon_{\text{Si}}}y_N\right) \tag{A11}$$

where the boundary condition $V(y_J + y_N) = V_{\text{sub}}$ was used to determine E_J from (A6). In terms of terminal voltages, E_J is

$$E_J = \frac{V_G - V_{FB} - {V_{\text{SiO}_2}}' - V_p' - V_n' - V_{\text{sub}}}{y_N + y_J + \left(\frac{\epsilon_{\text{Si}}}{\epsilon_{\text{SiO}_2}}\right)d} \tag{A12}$$

where

$${V_{\text{SiO}_2}}' \equiv \frac{qN_A y_J d}{\epsilon_{\text{SiO}_2}} \tag{A13}$$

$$V_p' \equiv \frac{qN_A}{2\epsilon_{\text{Si}}}{y_J}^2 \tag{A14}$$

$$V_n' \equiv \frac{qN_D}{2\epsilon_{\text{Si}}}{y_N}^2. \tag{A15}$$

$y_{\min}$, $V_{\min}$, and E_{SiO_2} are given by

$$y_{\min} = y_J + \frac{\epsilon_{\text{Si}}}{qN_A}E_J \tag{A16}$$

$$V_{\min} = V_J - \frac{qN_A}{2\epsilon_{\text{Si}}}(y_J - y_{\min})^2 \tag{A17}$$

$$E_{\text{SiO}_2} = \frac{qN_A y_{\min}}{\epsilon_{\text{SiO}_2}}. \tag{A18}$$

For the CCDs considered here, $y_N \gg y_J + (\epsilon_{\text{Si}}/\epsilon_{\text{SiO}_2})d$, and (3) results from (A11) and (A12). It also follows that if $y_N \gg y_J + (\epsilon_{\text{Si}}/\epsilon_{\text{SiO}_2})d$ then $N_D \ll N_A$ for the above derivation of potentials and fields to be valid. This can be seen from the the charge neutrality condition for field lines from the p-channel that terminate in the substrate just at full depletion, i.e.,

$$qN_A(y_J - y_{\min}) = qN_D y_N \tag{A19}$$

Fig. 17 compares the potential calculated from the above equations to a 1-D simulation (Medici 4.0.1). The simulation cross section shown in Fig. 1 was used and was generated from realistic process conditions that were input to the process simulator TSUPREM4. One-dimensional simulations were generated by biasing all phases in collection mode at −5 V. Good agreement between the simulation and analytic model is observed except in the region to the left of the potential minimum. The discrepancy in this region is due to the fact that

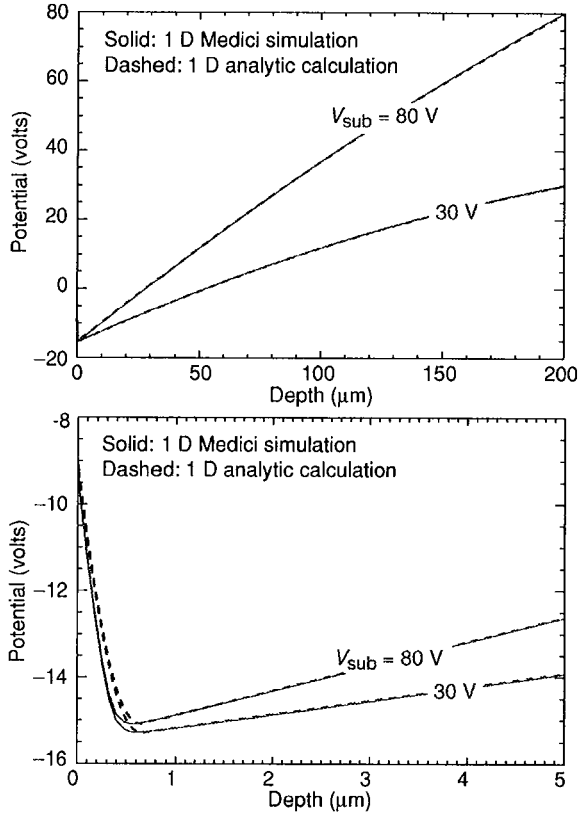

Fig. 17. Calculated and simulated potential versus depth for a CCD operated overdepleted. The calculations are based on the equations given in Appendix A, and the details of the 1-D simulation are described in the text. The calculations and simulations are nearly indistinguishable at the scale shown in the upper plot. The potential is plotted along the center line of the pixel.

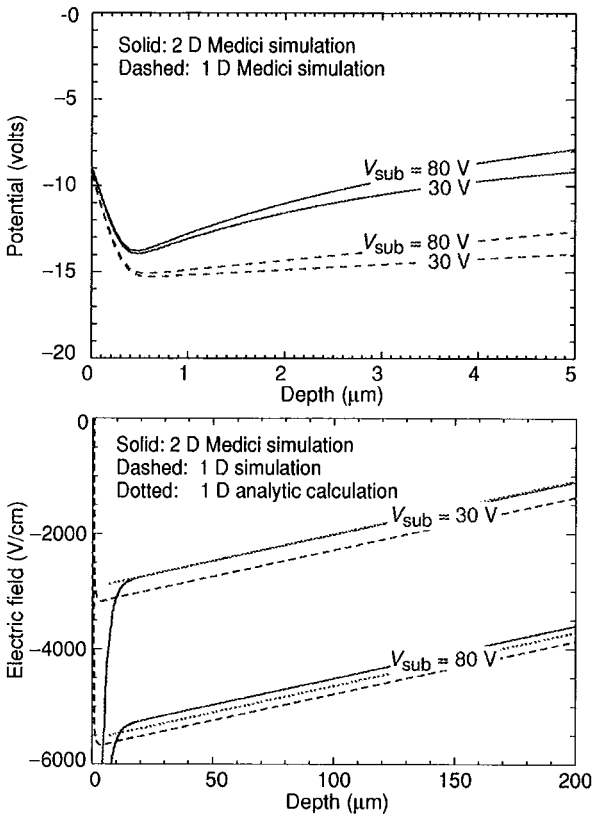

Fig. 18. Simulated potentials and electric fields versus depth for a CCD operated overdepleted. The dotted lines shown in the electric field plot were calculated from (A9) and (A11) with V_J and y_N adjusted to give a good fit for the 30-V case. The potential and field are plotted along the center line of the pixel.

the uniform channel doping assumed in the analytic model does not realistically describe the simulated implanted channel. In order to constrain the analytic model, it was required that the total integrated channel doping be the same as simulated (1.27×10^{12} cm^{-2}). The substrate doping and thickness were 6×10^{11} cm^{-3} and 200 μm, respectively, and the gate insulator was 41.7/50 nm SiO_2/Si_3N_4.

The interesting point to note from Fig. 17 is the near insensitivity of the potential minimum to the applied substrate bias as predicted by (3). As discussed above, this is a result of the thick depleted region and large difference in doping between the channel and the high-resistivity substrate. The charge neutrality condition for the overdepleted case derived from (A11) and (A16) with the substitution $V_n' + \Delta V$ for $V_{\text{sub}} - V_J$ is

$$(y_J - y_{\min}) = \frac{N_D}{N_A} y_N + \frac{\epsilon_{\text{Si}}}{qN_A} \frac{\Delta V}{y_N} \qquad \text{(A20)}$$

where $V_n' = qN_D y_N^2 / 2\epsilon_{\text{Si}}$ is the depletion voltage and ΔV is the voltage above full depletion. For typical values of N_D and N_A of 4×10^{11} cm^{-3} and 2×10^{16} cm^{-3}, respectively, (A20) predicts that only 0.6% of the field lines from the channel terminate in the substrate just at full depletion for y_J and y_N values of 1 and 300 μm, respectively. If the substrate is overdepleted by $\Delta V = 50$ V, only 1.7% of the field lines from the channel terminate in the substrate. Hence, in this example, nearly all the field lines from the channel terminate on the gate electrodes. The voltage drop across the channel, and therefore the potential minimum, is a weak function of the substrate bias voltage when $N_D \ll N_A$ and $y_N \gg y_J + (\epsilon_{\text{Si}}/\epsilon_{\text{SiO}_2})d$. The latter can be rewritten as $C_{\text{DEPL}} \ll C_S$ where $C_{\text{DEPL}} = \epsilon_{\text{Si}}/y_N$ is the capacitance of the fully depleted n region and C_S is the capacitance of the series combination of the channel and gate insulator capacitors (ϵ_{Si}/y_J and $\epsilon_{\text{SiO}_2}/d$, respectively). In this context, the coupling of the substrate bias to the channel is weak due to the capacitor voltage divider formed by C_{DEPL} and C_S.

One-dimensional simulations are compared to 2-D results in Fig. 18. For the 2-D case, the center gate electrode of Fig. 1 was held at -5 V while the other electrodes were biased in barrier mode at +3 V. Electric fields were calculated by numerical differentiation of the simulated potentials. The effect of the positive barrier potentials is to raise the potential minimum by about 1 V in this case and to increase the magnitude of the electric field over a depth of about 10 μm when compared to the 1-D case. As expected, the insensitivity of the potential minimum to the applied substrate bias is still observed in the more realistic 2-D case.

The electric field calculations are needed to model the spatial resolution. As seen in Fig. 18, the 1-D calculation overestimates the magnitude of the field. This can be easily corrected by adjusting V_J and y_N in (A9) and (A11). This correction is shown as the dotted curves in Fig. 18. As described in Section VI, this is a reasonable simplification to the spatial resolution problem

since negligible diffusion occurs in the high field region near the potential wells where the field is no longer described by (A11).

APPENDIX B
DERIVATION OF PSF FOR A BACK-ILLUMINATED CCD WITH A FIELD-FREE REGION

A back-illuminated photodiode array consisting of p^+ diodes on n-type silicon, with field-free thickness $L_{\rm ff}$ and total thickness (field-free and depleted depth) L_b, was considered in the Crowell and Labuda analysis [50]. Surface and bulk recombination are characterized by surface recombination velocity S and minority carrier lifetime τ. $L_o = \sqrt{D\tau}$ is the diffusion length.

The continuity equation was solved with electron–hole pair generation due to a sinusoidal light source yielding a generation term of

$$G(x,y) = \frac{N_0}{2}\alpha(1-R)(1+\cos(kx))\exp(-\alpha y) \tag{B1}$$

where N_0 is the peak photon flux, $k = 2\pi f$ where f is the spatial frequency, and R is the wavelength-dependent reflectivity, which can be determined from optical calculations [21].

The total hole flux $J_p(x)$ consisting of the hole diffusion current entering the depletion region plus the number of holes per unit time and area that are optically generated in the depletion region is given as

$$J_p(x) = \left(\frac{N_0}{2}\right)(\eta_0 + \eta_k\cos(kx)) \tag{B2}$$

where

$$\eta_k = (1-R)\left[\frac{\alpha L_k}{\alpha^2 {L_k}^2 - 1}\times\gamma - \exp(-\alpha L_b)\right] \tag{B3}$$

$$\eta_o = \eta_k\,|_{k=0} \tag{B4}$$

$$\gamma = \frac{2(\alpha L_k + SL_k/D) - (\beta_+ - \beta_-)\exp(-\alpha L_{ff})}{\beta_+ + \beta_-} - (\alpha L_k)^{-1}\exp(-\alpha L_{ff}) \tag{B5}$$

$$\beta_\pm = (1 \pm SL_k/D)\exp \pm\left(\frac{L_{ff}}{L_k}\right) \tag{B6}$$

$$\frac{1}{{L_k}^2(k)} = \left(\frac{1}{{L_o}^2}\right) + k^2. \tag{B7}$$

Note that η_o models the QE in the presence of surface and bulk recombination for the case of a field-free region at the back surface. A further refinement to the basic QE model including an electric field at the back surface was given by Blouke *et al.* [49].

In order to simplify the above, we first neglect bulk recombination. This results in $1/L_k(k) \approx k$ with β now given by

$$\beta_\pm \approx (1 \pm S/(Dk))\exp \pm(kL_{\rm ff}). \tag{B8}$$

We further assume that the absorption length is small compared to $L_{\rm ff}$, so that $\alpha L_{\rm ff}$ and αL_b are large. Hence the exponential terms in (B3) and (B5) are neglected, and γ becomes

$$\gamma \approx \frac{2\alpha}{k(\beta_+ + \beta_-)} + \frac{S}{Dk(\beta_+ + \beta_-)} \tag{B9}$$

and substitution into (B3) yields

$$\frac{\eta_k}{(1-R)} \approx \frac{2}{\beta_+ + \beta_-} + \frac{S}{\alpha D(\beta_+ + \beta_-)} \tag{B10}$$

where the approximation $\alpha^2 L_k^2 \approx \alpha^2/k^2 \gg 1$ was used (valid for the spatial frequencies of interest, i.e., $\approx$ Nyquist and below). The MTF neglecting surface recombination is then

$$\mathrm{MTF}_{\rm ff} = \frac{\eta_k}{\eta_o} \approx \frac{1}{\cosh(kL_{\rm ff})}. \tag{B11}$$

This result can be derived from Barbe's equation [56, eq. 83]

$$\mathrm{MTF}_{\rm ff} \approx \frac{\cosh\left(\frac{L_{\rm ff}}{L_o}\right)}{\cosh\left(\frac{L_{\rm ff}}{L_k}\right)} \tag{B12}$$

for the case of negligible recombination.

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A Low Power, Wide Dynamic Range Multigain Signal Processor for the SNAP CCD

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Abstract—**A four-channel custom chip designed for reading out the CCDs of the proposed SNAP satellite visible imager is presented. Each channel consists of a single-ended to differential converter followed by a correlated double sampler and a novel multislope integrator. The output signal is differentially brought out of the chip by an output buffer. This circuit is designed to operate at room temperature for test purpose and at 140 K, which will be the operating temperature. The readout speed is 100 kHz. The 16-bit dynamic range is covered using 3 gains each with a 12-bit signal to noise ratio. The prototype chip, implemented in a 0.25 μm CMOS technology, has a measured readout noise of 7 μV rms at 100 kHz readout speed, a measured nonlinearity of $\pm$0.0025% and a power consumption of 6.5 mW, with a 3.3 V supply voltage.**

Index Terms—**Analog processing circuits, charge coupled devices, CMOS analog integrated circuits, correlated double sampling.**

I. Introduction

A four-channel custom chip designed for reading out charge coupled devices (CCDs) is presented. This design is part of the research and development program for the Super Nova/-Acceleration Probe (SNAP) project. SNAP is an international satellite proposal dedicated to understanding the dark energy responsible for the accelerating expansion of our universe. It has a 2 meters telescope with a large field of view. CCDs and near-infrared detectors are located on the focal plane for imaging and spectroscopy. The primary goal of this circuit is to cover a 16-bit dynamic range with a readout noise of 7 μV rms (2 electrons) referred to the input at 100 kpixel/s readout speed. The operating temperature of 140 K is needed to lower the detector dark current.

The circuit described is intended to operate close to the CCDs in order to avoid long cable connections and minimize pick-up noise. This gives additional constraints to the circuit such as low power consumption, operation at 140 K and radiation tolerance to a total dose of 10 krad. This paper is organized as follows. In Section II, the signal processing method used in this design is described. The circuit architecture and the principle of operation are presented in Section III. Detailed descriptions of some critical blocks are presented in Section IV. Section V is devoted to simulation results and chip layout is discussed in Section VI. Experimental results are presented in Section VII.

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II. Signal Processing Method

The output signal from a CCD needs to be processed to remove the reset level, reduce the noise and accommodate the dynamic range before being digitized.

A. Noise Study

Several types of signal processing methods suitable for optimizing the signal over noise ratio of a CCD are reviewed in [1]. SNAP plans to use the LBNL high resistivity, p-channel CCD. This device has a noise spectral density at the output stage with a thermal noise component of 20 $\mathrm{nV/Hz^{1/2}}$ and a 1/f noise of 1.5 $\mu\mathrm{V/Hz^{1/2}}$ at 1 Hz with a frequency exponent of 1. According to [1], the most appropriate technique is the differential averager which consists of a correlated double sampler (CDS) followed by an integrator, as the thermal noise level of the CCD is high. This technique was simulated by injecting modeled noise spectral densities of the dominant noise sources into a behavioral model. These are the CCD source follower output stage and the front-end circuit input stage. The block diagram of this model is shown in Fig. 1. The first stage converts the single ended input signal to a differential signal with a voltage gain of 4, using two ideal operational amplifiers labeled A1 and A2 with resistive feedback. A switch matrix is used to implement the correlated double sampling function. The last stage is an ideal differential integrator. The spectral noise density labeled V_n of the amplifiers A1, A2, and A3 has a thermal noise level of 4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and a 1/f noise of 1 $\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ at 1 Hz with a frequency exponent of 1. This spectral density is a model of an input differential pair biased with a tail current of 200 μA and an aspect ratio of 1000. The CCD noise source is also injected at the input with the spectral density described above. Transient noise analysis was performed using the Eldo simulator tool [2], with an integration time $T = 2\tau$ of 8 μs. The CCD noise contribution is 10 μV rms while the front-end noise contribution is 6.3 μV rms, both referred to the input. Hence, the total noise referred to the input noise is 12 μV, which is the square root of the quadratic sum of the CCD noise and the front-end noise.

These results are in a good agreement with the equations developed in [1]. The conversion gain of the CCD is 3.5 μV/e. The noise requirement for the focal plane is 4 electrons rms for a readout frequency of 100 kHz. The simulation results give a total noise of 12 $\mu\mathrm{V}/3.5\ \mu\mathrm{V/e} = 3.4$ e rms which meets the requirements with some margin.

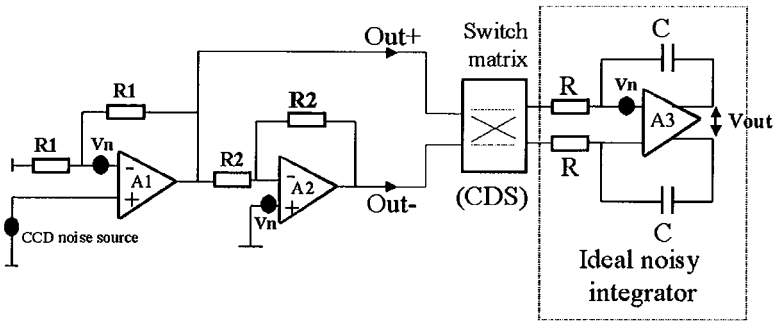

Fig. 1. Behavioral model used to simulate the noise contribution of the CCD and front-end circuit filtered by a differential averager.

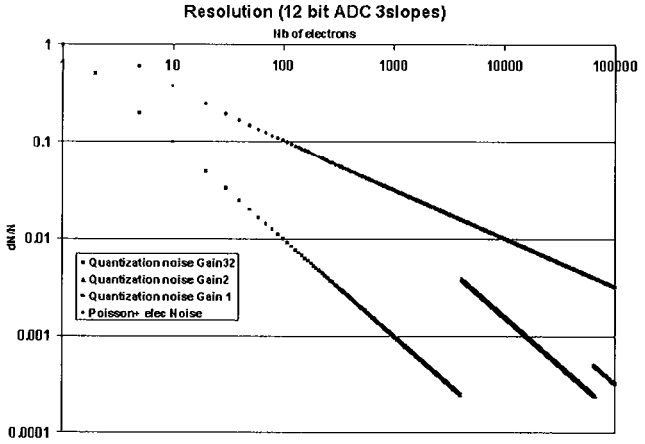

Fig. 2. Resolution dN/N referred to the input as a function of the input signal N for the Poisson process, the quantization and electronic noise contribution. A 12-Bit resolution ADC and an integrator gain of 32, 2, and 1 are assumed in this case.

B. Dynamic Range

The dynamic range requirement is 16-bit, from 2 electrons to 130 k electrons. However, the requirement for the S/N is driven by the Poisson process of the light interacting in the sensor which has a variance equal to N, where N is the number of incoming photons [3]. The signal can be digitized with an LSB size that depends on the signal amplitude such that the ADC quantization noise is still below the Poisson noise. This concept has been implemented on chip using a novel 3-slope multirange integrator with voltage gains of 32, 2, and 1 for a given integration time. In this case, a 12-bit resolution ADC is sufficient, and the quantization noise referred to the input is 1 electron for an integrator gain of 32. Fig. 2 shows the contributions of the Poisson process, the electronic noise and the quantization noise to the resolution dN/N referred to the input, as a function of the signal amplitude N. The resolution dN/N due to the Poisson process and the electronic noise is given by

$$\frac{dN}{N} = \sqrt{\left(\left(\frac{N_{el}}{N}\right)^2 + \left(\frac{1}{N}\right)^2\right)} \tag{1}$$

where, $N_{el} = 1.8$ e rms is the front-end noise.

The resolution dN/N due to the quantization noise is given by

$$\frac{dN}{N} = \frac{N_{fs}}{NG2^n} \tag{2}$$

where N_{fs} is the full scale signal, G is the integrator gain and n the number of bits.

III. Channel Architecture

The differential averager technique depicted in Fig. 1 along with a novel 3-slope multirange integrator accommodating the 16-bit dynamic range with a 12-bit resolution was implemented on a chip. The block diagram of one channel is shown in Fig. 3 and the associated timing diagram is shown in Fig. 4.

The channel consists of a single-to-differential converter followed by a correlated double sampler (CDS) and a multirange gated integrator. The output signal is differentially brought out of the chip by two output buffers. The CCD is AC-coupled to the input of the channel. A clamp switch, controlled by the signal labeled "clamp," restores the input baseline to a fixed potential V_{ref} during the CCD reset phase. The CDS subtracts the low frequency noise, the CCD pixel reset level, and the offset from the single-to-differential stage.

The multirange integrator consists of a fully differential operational transconductance amplifier (OTA) fed back by an RC network setting the integrator gain. Depending on the capacitance value, the integrator has a gain of 32, 2 or 1. A pair of first-order charge injection compensated switches in series with the resistance control the integration time. The multirange operation is as follows. After resetting the integrator (reset switches not shown on the figure), the integrator switch, controlled by the signal labeled "integrate control," is turned on and the CCD reset level is integrated for 4 μs. During the next 1 μs, the switch is turned off and the integrator is insulated from the CDS operation (controlled by the signal labeled "CDS ctrl") and input signal transient, without disturbing the charge already stored in the feedback capacitors. Once the input signal is settled, the integration starts again for 4 μs. At the beginning the default gain setting is 32. A logic circuitry automatically switches to the gain 2 and 1 if the output signal exceeds a threshold. This threshold is set to 80% of the full scale. The logic provides two signals labeled "slope1" and "slope2" indicating the integrator gain at the end of the processing cycle. Besides the automatic gain change mode, each gain can be forced individually. A signal labeled "veto" disables the logic circuitry 500 ns before the end of the signal integration time, to avoid any gain changes just before stopping the integration. The data is ready to be digitized a couple of hundred ns after the end of the signal integration time (position labeled ADC in Fig. 4). Two buffers

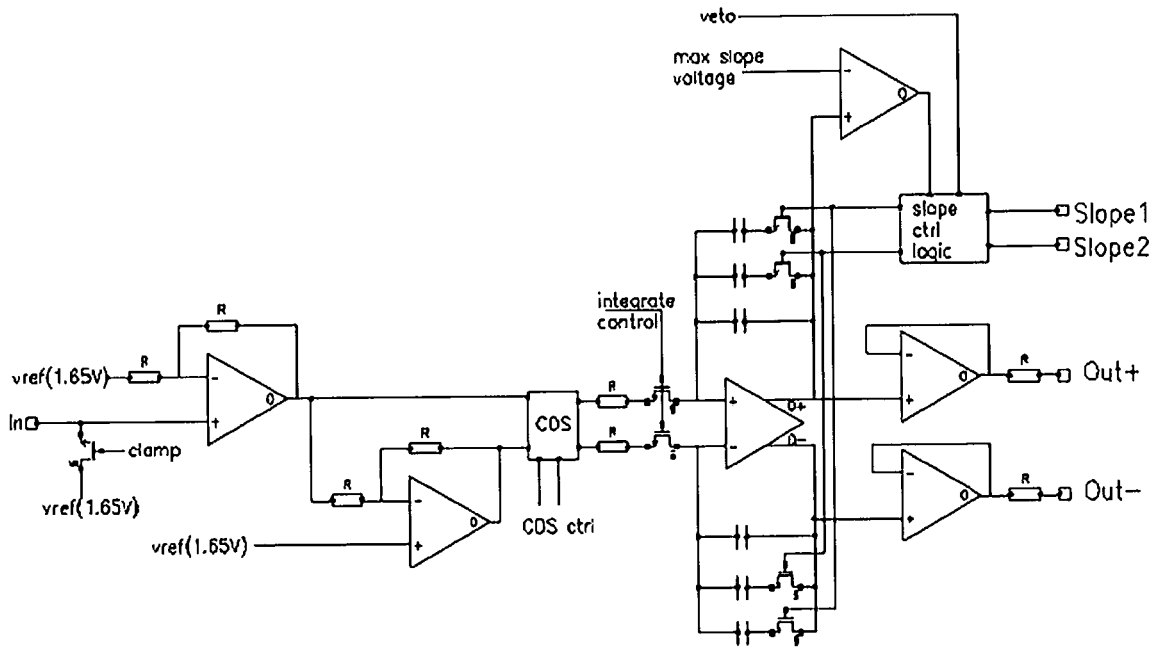

Fig. 3. Channel block diagram.

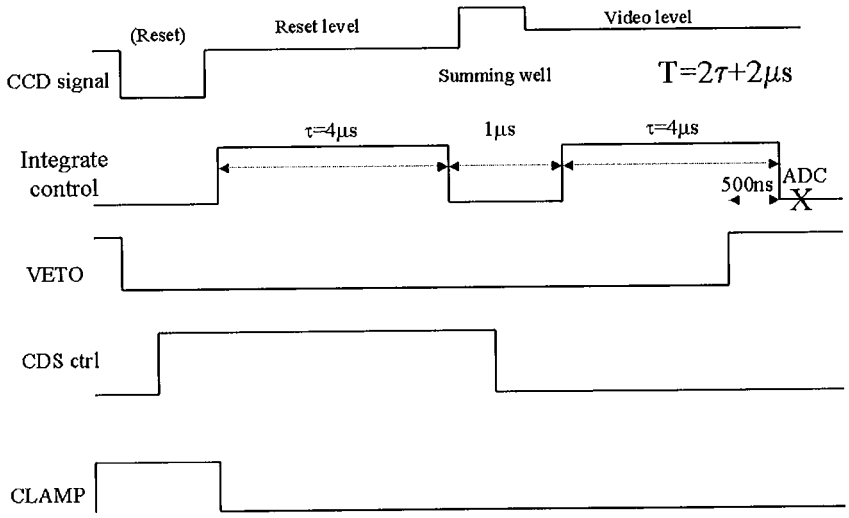

Fig. 4. Timing diagram.

are connected to the positive and negative outputs of the integrator to drive off-chip circuitry.

IV. Circuit Description

This section focuses on more detailed circuit descriptions of the sensitive parts of the design linked to the circuit performance needed. This concerns particularly the multirange integrator.

A. Single-to Differential Converter and Correlated Double Sampler

The full-scale input signal is typically +500 mV. The single-to-differential stage has a gain of 4 in order to reduce the noise contribution of the integrator. A 500 mV full-scale signal generates a 2 V differential signal, at the input of the CDS, with a common mode component at $V_{dd}/2$. The amplifiers have large DC gain (120 dB) in order to achieve good linearity when the signal is settled (reset and signal plateau). The settling time is about 200 ns to achieve 16-bit linearity. The opamp employed in this design has a conventional folded cascode input stage [4] followed by a Miller-compensated class A/B stage [5]. An enhanced slew rate source follower [6] is used as the opamp output stage in order to drive the resistive feedback network. The opamp input differential pair is biased with a tail current of 200 μA, achieving a thermal noise spectral density of about 4 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and has an aspect ratio of a 1000.

The CDS has a four-switch matrix. The on resistance of these switches depends on the signal amplitude as they are in series with the integrator resistor. Care has been taken to size them

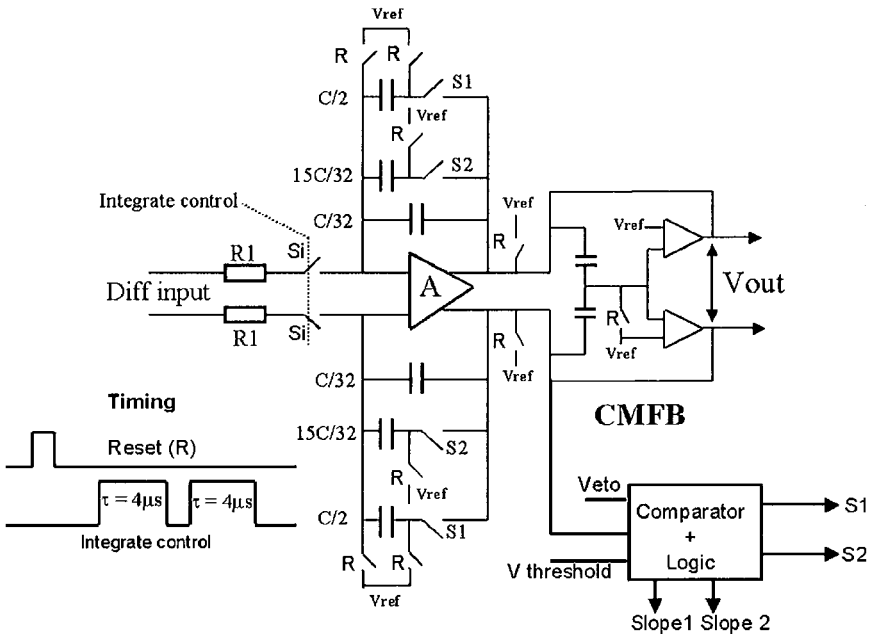

Fig. 5. Multislope integrator.

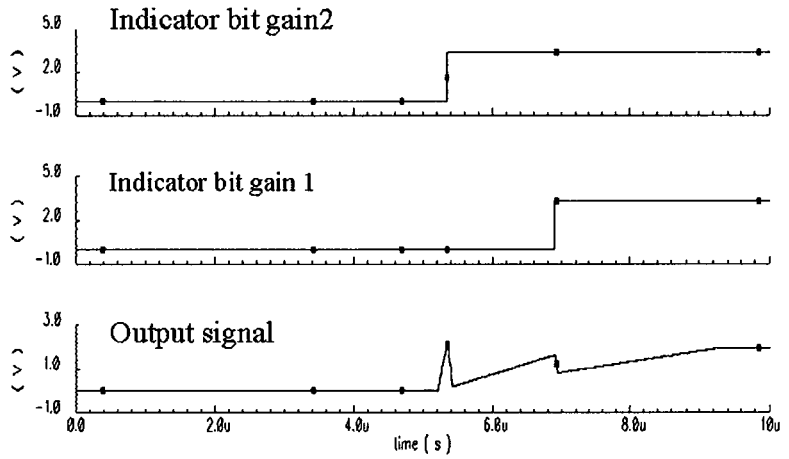

Fig. 6. Slope indicator bits and analog output signal of the channel for a full scale input signal of 500 mV. The readout cycle is 10 μs.

such that their on resistance variation over the full signal range is a small fraction of the total integrator resistance value ($\leq$0.02%) to keep the linearity.

B. Multirange Integrator

The multislope integrator schematic is depicted in Fig. 5. A bank of capacitors in the feedback along with the resistor R1 set the integrator gain to 32, 2 or 1 depending on the S1 and S2 switch settings. The resistance R1 is 50 kΩ and the total capacitance in the feedback is 2.5 pF, 40 pF or 80 pF. The amplifier labeled A is a conventional fully differential single-stage folded cascode OTA [7]. The degenerated differential input pair is biased with a tail current of 400 μA.

A dynamic switched capacitor common-mode feedback circuit (CMFB) senses and sets the common-mode voltage at the integrator output [8]. During the reset period, the switches labeled R set the common mode voltage to V_{ref} ($V_{dd}/2$) at both the input and output and discharge the feedback capacitors. Once the reset switches R are turned off, the common-mode feedback circuit controls the common voltage at the output. The switches S_i start and stop the signal integration. A single stage comparator followed by a Schmitt trigger senses and compares the output signal to $V_{threshold}$. If it exceeds the threshold voltage, the switch S_2 is turned on first, changing the gain from 32 to 2. If the output signal is again above threshold, the switch S_1 is turned on and the gain becomes 1.

During the switching time, a charge error is introduced because the OTA virtual ground moves. This error is constant as we are switching from one slope to another with the same output signal amplitude. The integrator output voltage is digitized when the integration is done and then the OTA virtual ground is equal to the output voltage divided by the DC gain (hold mode). Charge injection from the S_i switches creates a small common mode voltage variation. A dummy switch connected in series is used to reduce this effect.

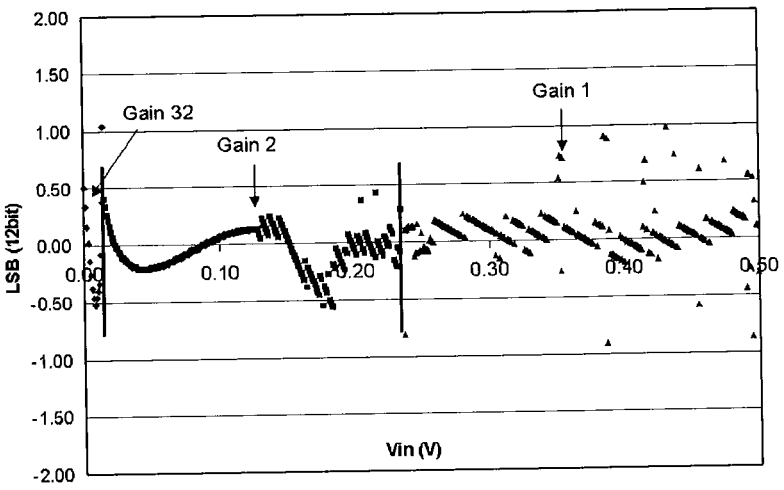

Fig. 7. Simulated nonlinearity of the channel as a function of the input signal, over the 3 ranges. The readout cycle is 10 μs. The saw-tooth structure is an artifact of the simulator numerical precision.

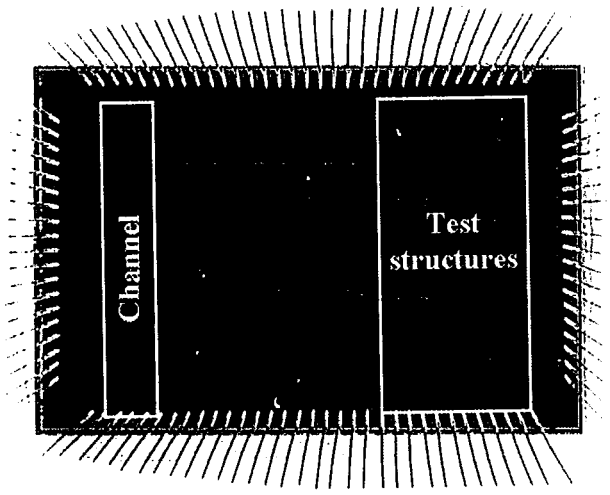

Fig. 8. Photograph of the prototype chip.

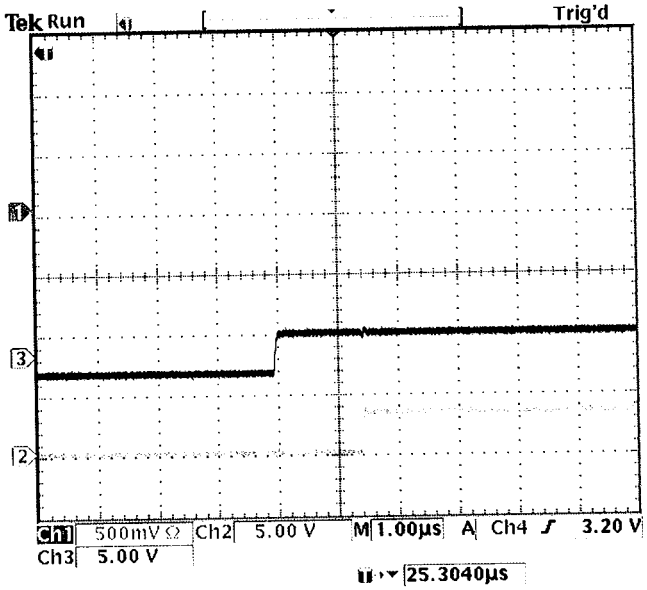

Fig. 9. Channel output signal and gain change indicator bits for a large input signal. The readout cycle is 10 μs. ADC conversion occurs at the far right of the top trace.

V. Simulation Results

The circuit was extensively simulated using the Eldo simulator tool. Typical and corners model parameters were used for simulation at both 300 K and 140 K. At 140 K, the threshold voltage of transistors is increased by 160 mV for both N and P type. The carrier mobility also increases by a factor of 1.7 for both NMOS and PMOS compared to room temperature. This effect can have an impact on the linearity and stability of the active parts and has been taken into account. Model parameters were adjusted according to measurements we have performed on test transistors.

Fig. 6 shows the simulated output signal of the channel for a full-scale input voltage of 500 mV. The readout cycle is 10 μs. The two upper traces are the slope indicator bits, indicating two gain changes as expected. The bottom trace shows the integrator output through the output buffer. Fig. 7 shows the simulated deviation from the best-fit line of the channel as a function of the input signal over the 3 ranges. A simulated nonlinearity of ± 1 LSB (12-Bit) is obtained at both 300 K and 140 K.

Noise simulations in the time domain using the transient noise analysis of the Eldo simulator were performed on the channel. The input referred noise level is 7 μV rms at 300 K and 5.6 μV at 140 K. As the CCD conversion gain is 3.6 μV/e, the corresponding input referred noise in electrons is 2 and 1.6, respectively.

VI. Chip Layout

The prototype chip is implemented in a commercial 0.25 μm mixed-mode CMOS technology. The die size is 3.6 mm $\times$ 5.4 mm. A photo of the die is shown in Fig. 8. The chip contains 4 channels along with stand-alone building blocks such as the single-to-differential converter and the multirange integrator for test purposes.

VII. Experimental Results

The prototype chip is packaged in a 120-pin CERQUAD package and has been tested using a 16-bit resolution test board,

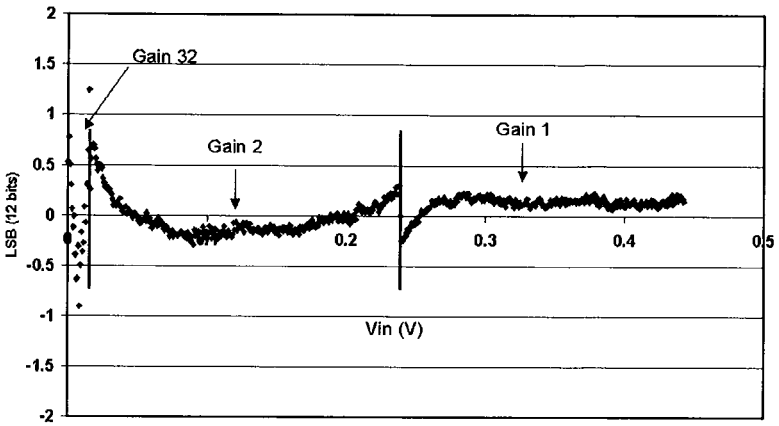

Fig. 10. Measured nonlinearity as a function of the input signal at 300 K.

TABLE I
SUMMARY OF THE CHANNEL PERFORMANCES AT 300 K

Parameter	Value
Dynamic range	16-bit
Noise (100KHz readout rate)	7μV rms (2e)
Noise (50KHz readout rate)	5.25μV rms (1.5e)
Non-linearity	±1LSB (12-bit)
PSRR	74 dB (100KHz)
Gain temperature coefficient	400ppm/K

TABLE II
SUMMARY OF THE CHANNEL PERFORMANCES AT 140 K

Parameter	Value
Noise (100KHz readout rate)	5.6μV rms (1.6e)
Noise (50KHz readout rate)	4.65μV rms (1.33e)
Non-linearity	±0.6LSB (12-bit)
PSRR	74 dB (100KHz)
Gain temperature coefficient	400ppm/K

including digital to analog converters (DACs) to inject signal at the input and analog to digital converters (ADCs) to digitize the signal at the output. A pattern generator provides LVDS control signal to the chip. The operation of the circuit is verified with a supply voltage range from 3.1 V to 3.3 V. All results given are obtained with a 3.3 V supply unless otherwise specified. The reference voltage V_{ref} needed to set the common voltage of the channel is set to 1.65 V ($V_{dd}/2$). The performance of the chip is measured at room temperature and at 140 K by using a tailored test board in a liquid nitrogen cooled dewar.

A. Nonlinearity Measurement

Fig. 9 shows the integrator output for a large signal applied at the input (upper trace) along with the two gains change indicator bits (lower traces). A linearity measurement has been performed by injecting an input signal generated by the DAC ranging from 0 to full-scale at a read rate of 100 KHz. The deviation from the data and a best-fit line has been extracted over the three gains and is shown in Fig. 10. The measured nonlinearity is ±1 LSB (12-bit) at 300 K and ±0.6 LSB at 140 K. With a 3.1 V supply at 140 K, the measured nonlinearity is ±1.25 LSB.

B. Noise Measurement

A set of noise measurements at both temperatures was done by histograming the output voltage and calibrating the channel to get the exact conversion gain. A noise of 7 μV rms (2 electrons) referred to the input was measured at 100 kpixel/s readout rate and 300 K. At 140 K, the measured noise decreases by 20% with an rms value of 5.6 μV (1.6 electrons) as expected.

C. Measurements Summary

A summary of the achieved channel performances at 300 K and 140 K is shown in Table I and Table II, respectively. The measured power consumption is 6.6 mW. A signal-dependant cross talk between channels has been observed on the prototype. A common bus supplying the 1.65 V reference voltage on Fig. 3 creates a common mode coupling on the other channels. This effect has been identified in simulation and will be corrected in the next version.

VIII. CONCLUSION

A 16-bit linear multigain signal processor for the SNAP CCD has been achieved using a novel 3-range integrator each with a 12-bit signal to noise ratio. Crucial parameters such as power consumption, noise, linearity and operation at 140 were studied to obtain a reliable design. Experimental tests were performed to assess the performance of the circuit. We are now integrating the circuit with a CCD for a system test at 140 K to verify the signal processing efficiency with respect to the noise.

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Page last updated
July 23, 2009

BEAMLINE 5.3.1

Femtosecond Phenomena

Operational	Now
Source characteristics	Bend magnet
Energy range	1.8-12 keV (monochromatic)
Monochromator	White light and double crystal Si(111), Ge(111), or InSb(111)
Flux (1.9 GeV, 400 mA)	~1 x 10^{12} photons/s/3x10^{-4}BW
Resolving power (E/ΔE)	1200 at 5000 eV
Detectors	Picosecond streak camera and avalanche photodiode; spectrometer (resolving power ~500) covering ~250 eV—1 keV
Spot size at sample	100 x 300 μm
Samples	
Format	Crystals, liquid jets, foils
Sample environment	10^{-6} Torr vacuum or helium
Experimental techniques	Laser-/electron-beam modulation, time-resolved (subpicosecond) x-ray diffraction and absorption
Local contact/spokesperson	Rich Celestre Affiliation: Advanced Light Source, Berkeley Lab Phone: (510) 495-2053
Beamline phone number	(510) 495-2053

Table of all beamlines
Diagram of all beamlines